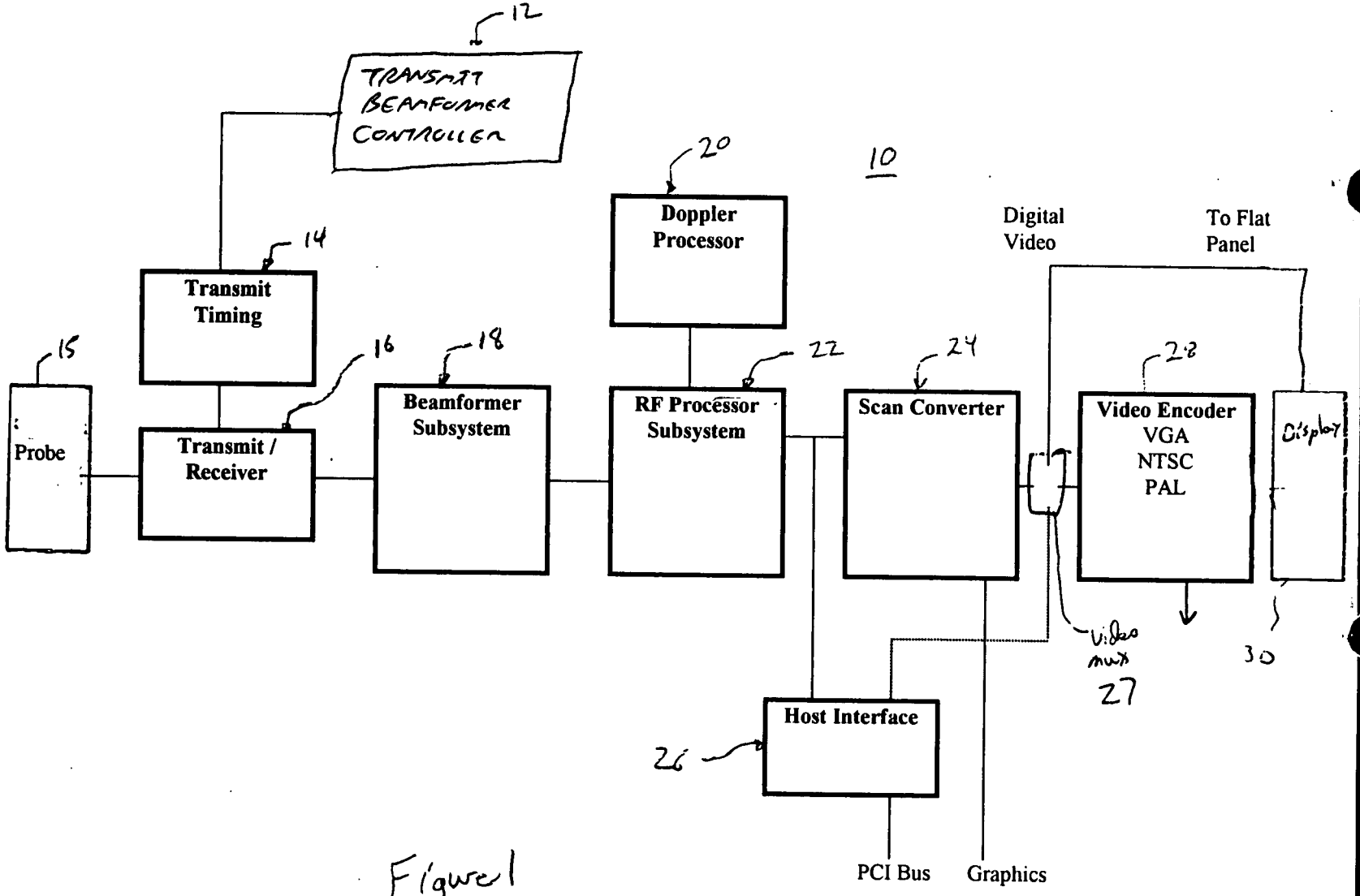

12
TRANSMIT BEAMFORMER CONTROLLER
10
20
Doppler Processor
Digital Video
To Flat Panel
14
Transmit Timing
15
Probe
16
Transmit / Receiver
18
Beamformer Subsystem
22
RF Processor Subsystem
24
Scan Converter
28
Video Encoder
VGA
NTSC
PAL
Display
Video mux
27
30
26
Host Interface
PCI Bus
Graphics

Figure 1

6,611,680 "98,96,20

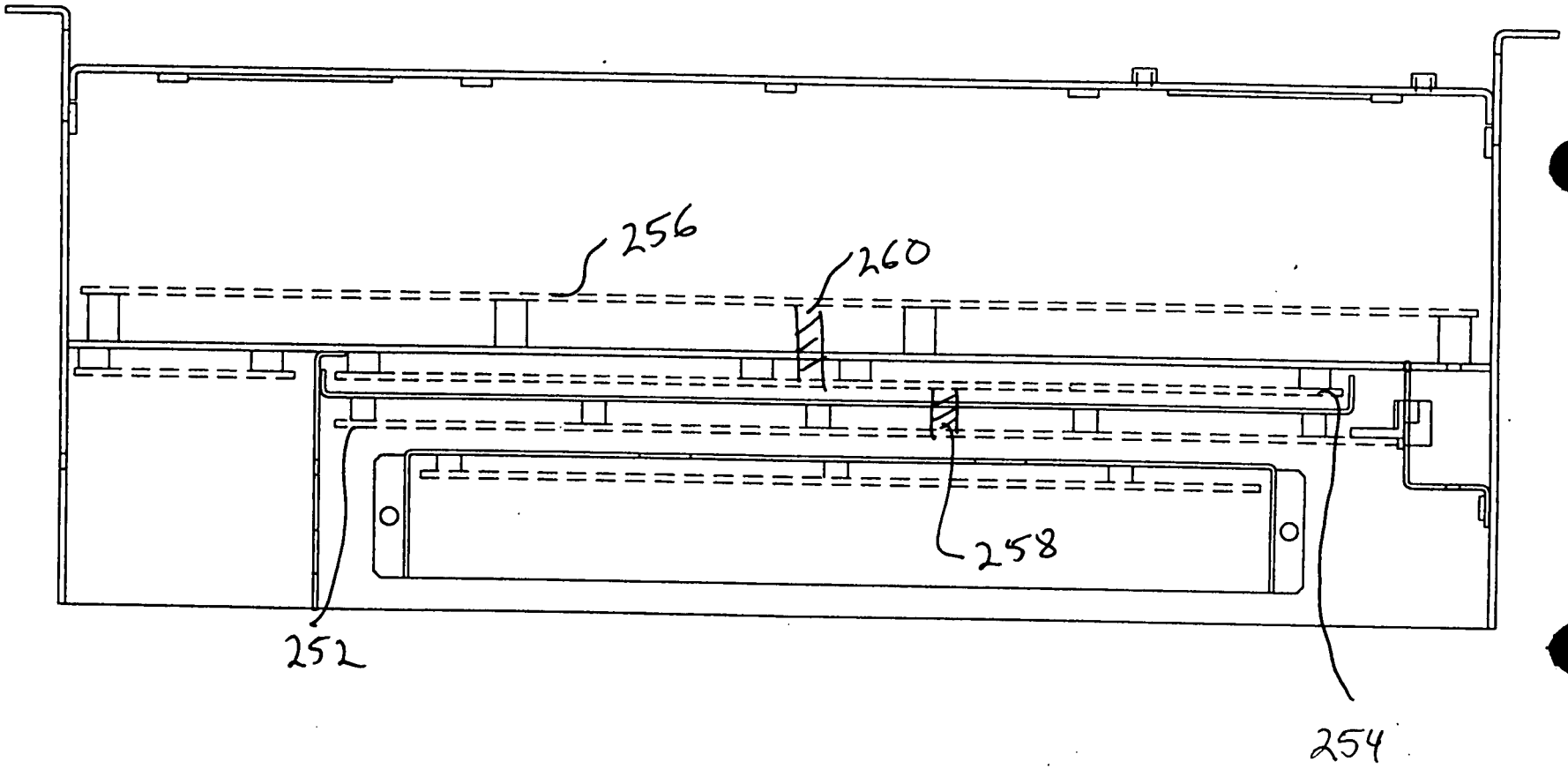


FIG 2

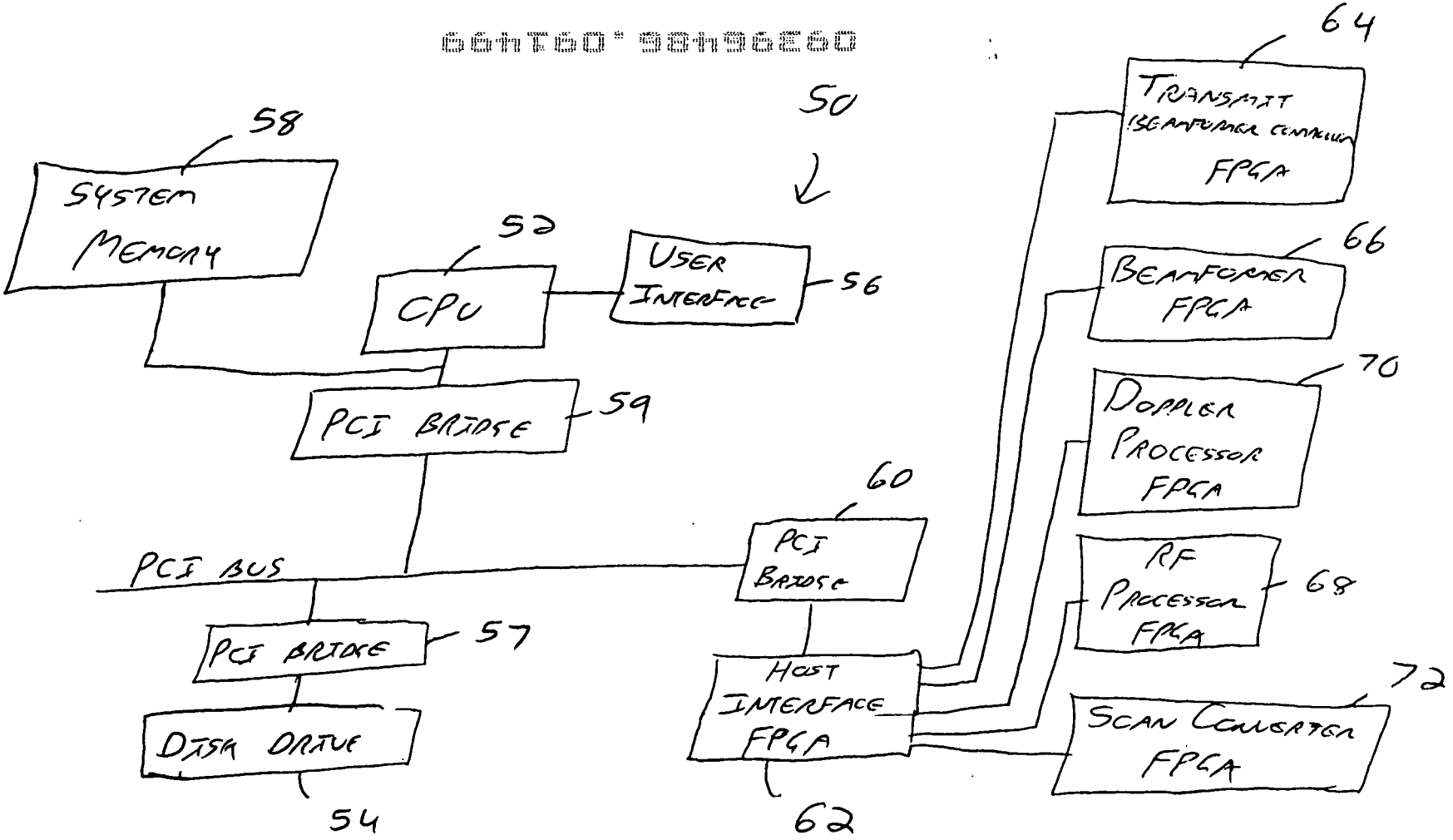

50
58
SYSTEM MEMORY
52
CPU
USER INTERFACE
56
PCI BRIDGE
59
PCI BUS
PCI BRIDGE
57
DISK DRIVE
54
60
PCI BRIDGE
HOST INTERFACE FPGA
62
64
TRANSMIT (BEAMFORMER CONTROL) FPGA
66
BEAMFORMER FPGA
70
DOPPLER PROCESSOR FPGA
RF PROCESSOR FPGA
68
72
SCAN CONVERTER FPGA

FIGURE 3

FIG 4A

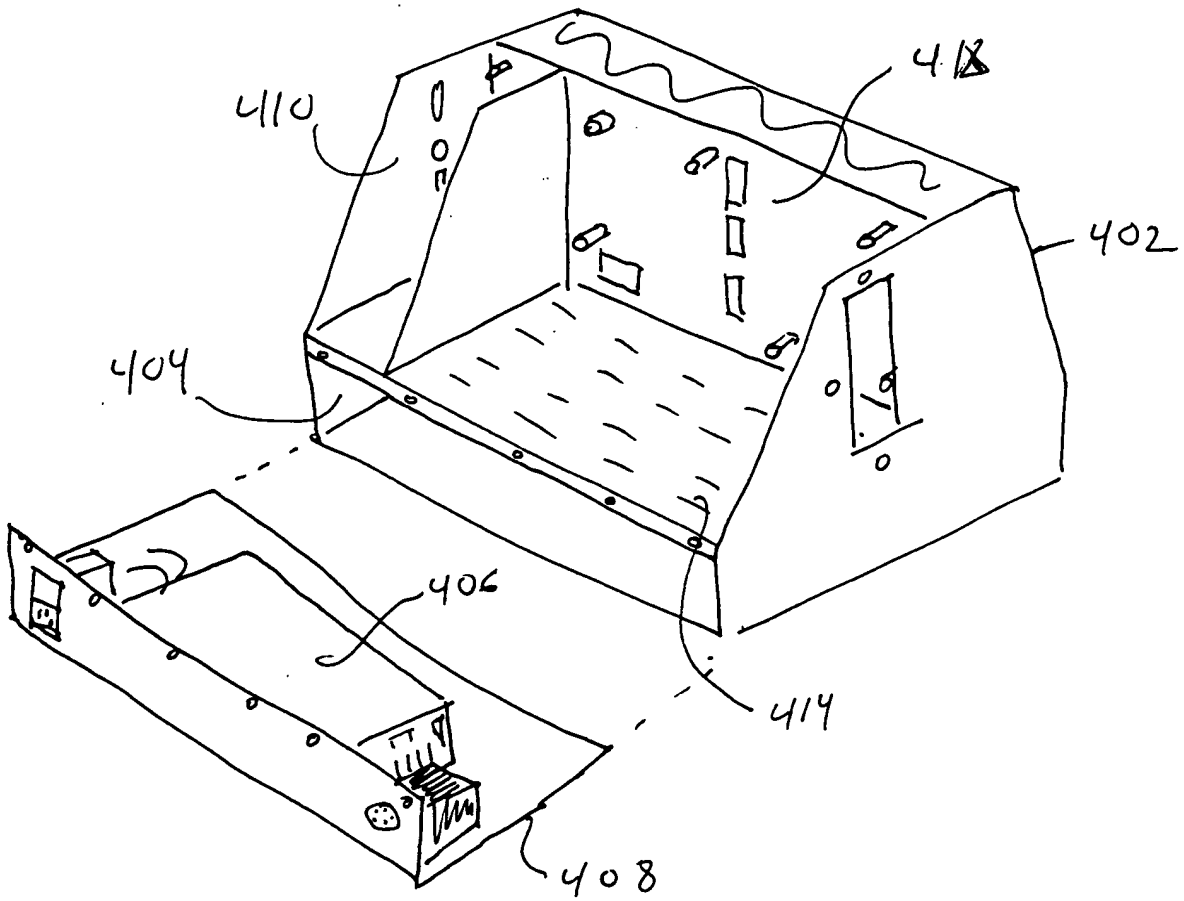
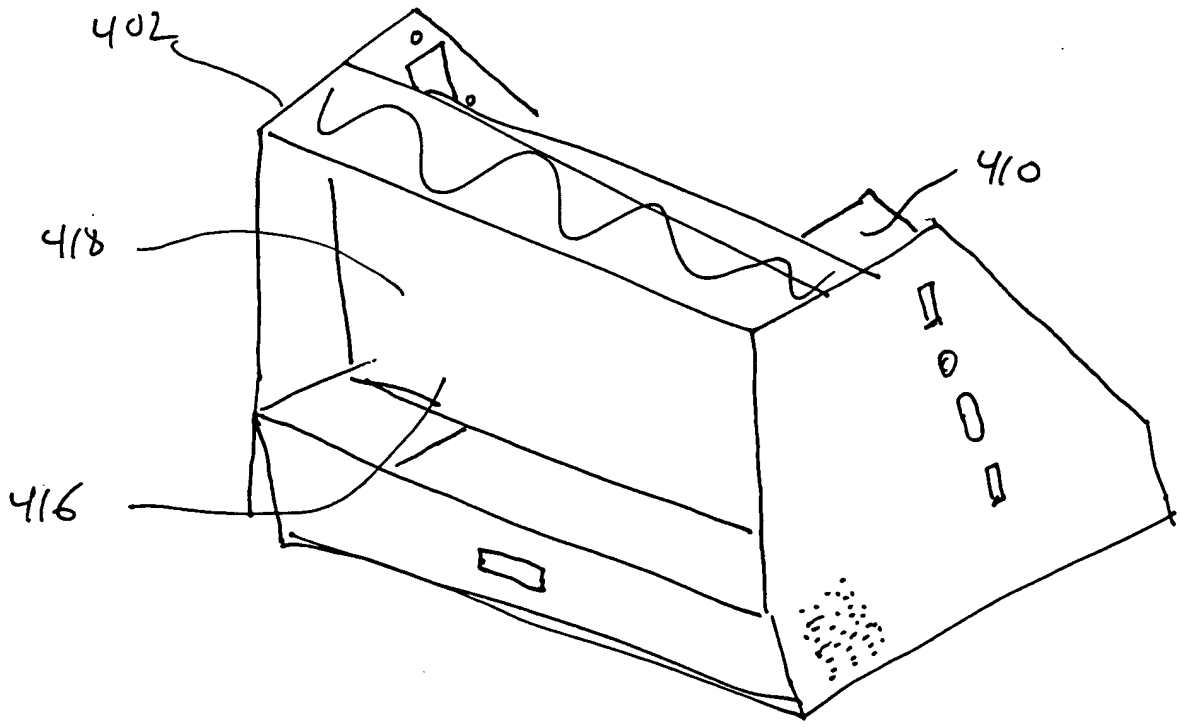


FIG 4B



Docket No. 50269-0045

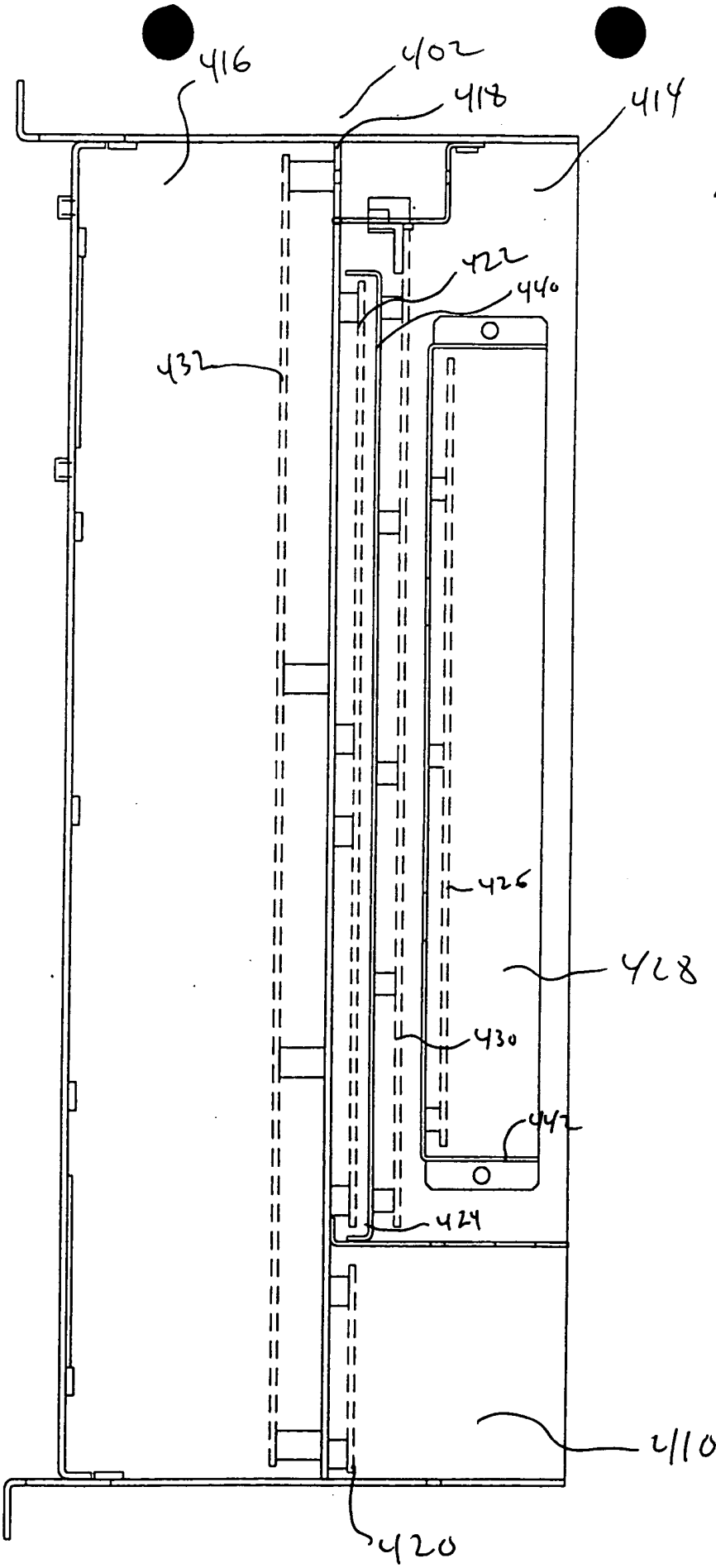


FIG 4C

FIG 4D

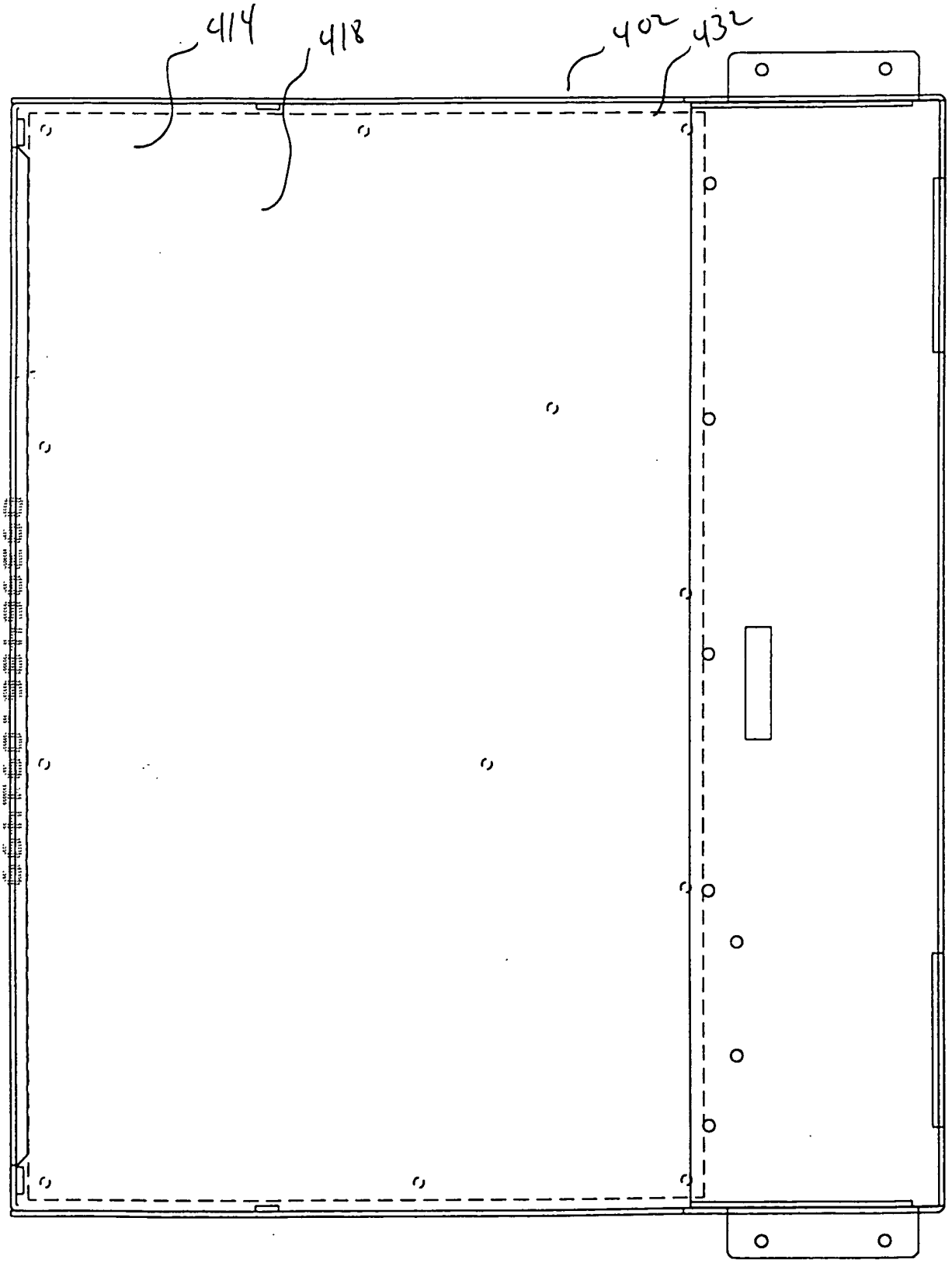


FIG 4E

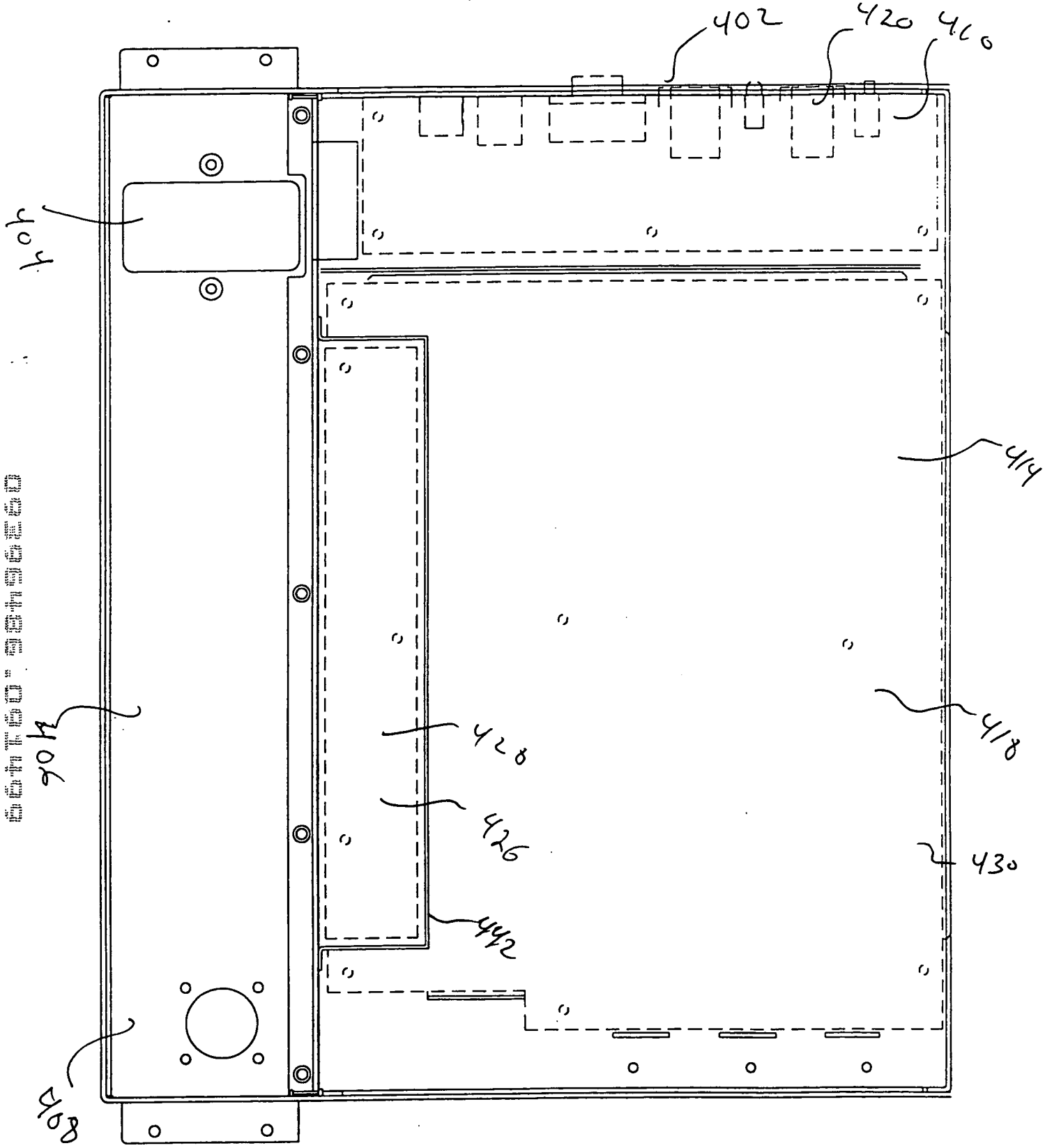


FIG 4F

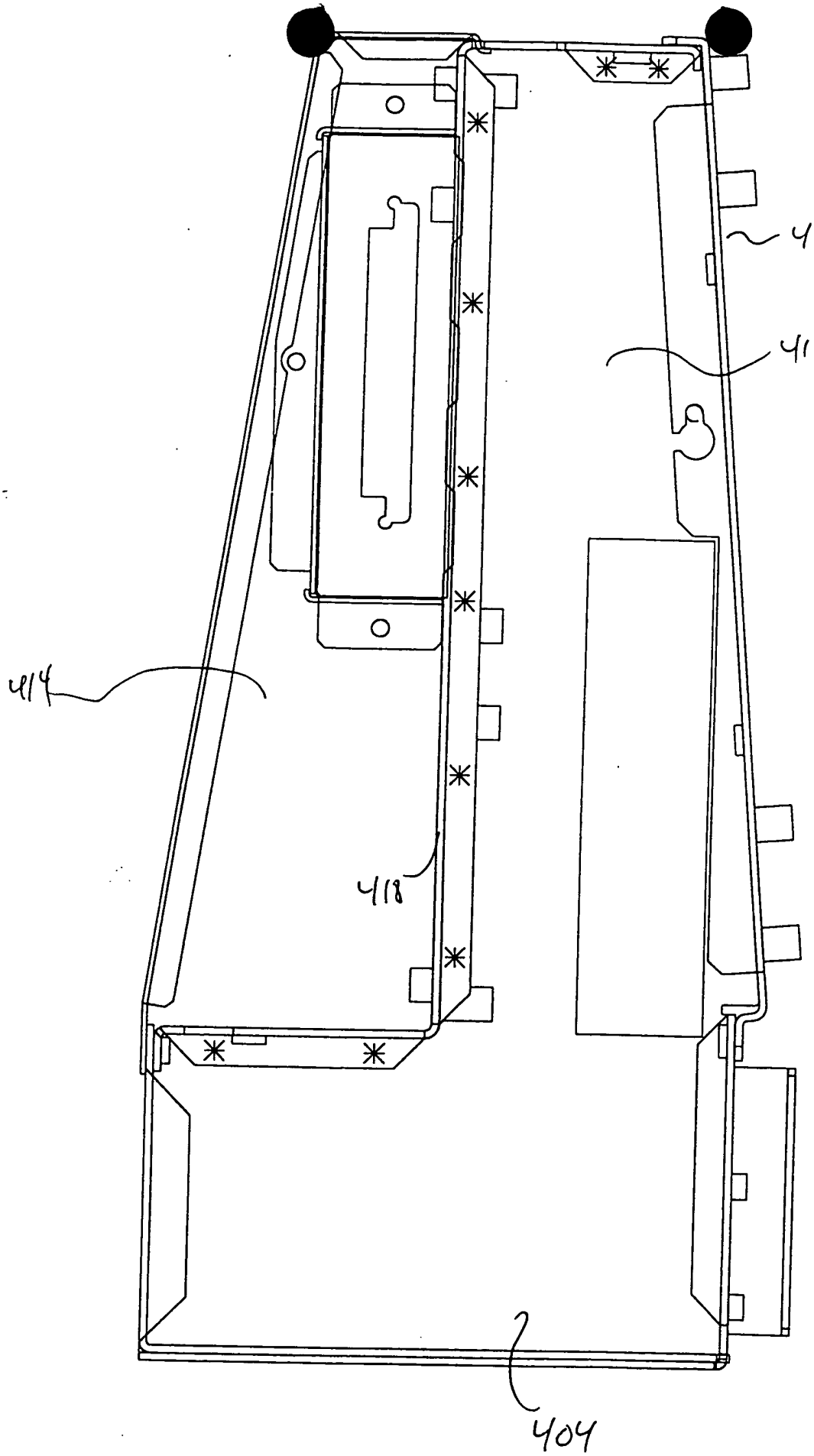


FIG 4G

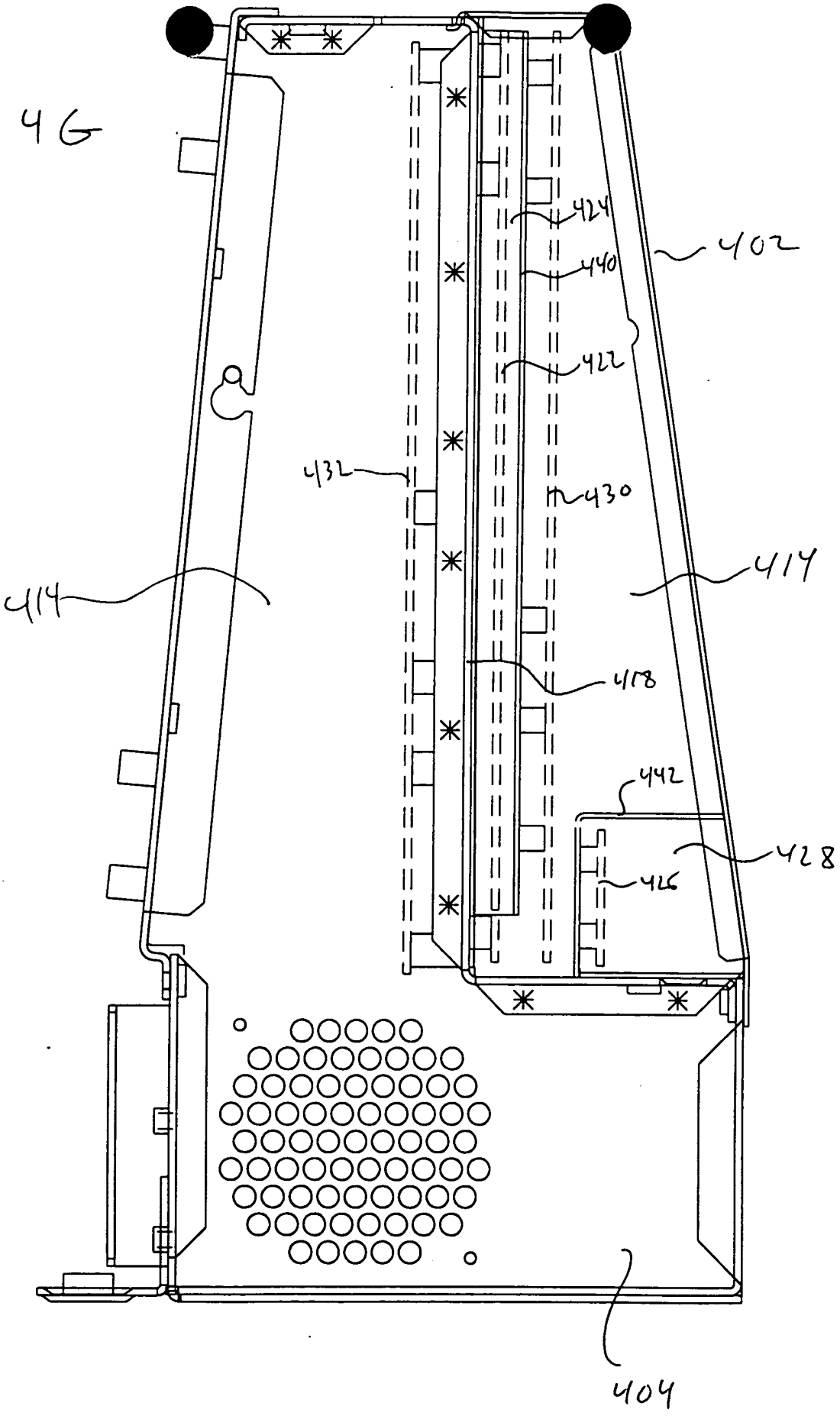


FIG 4H

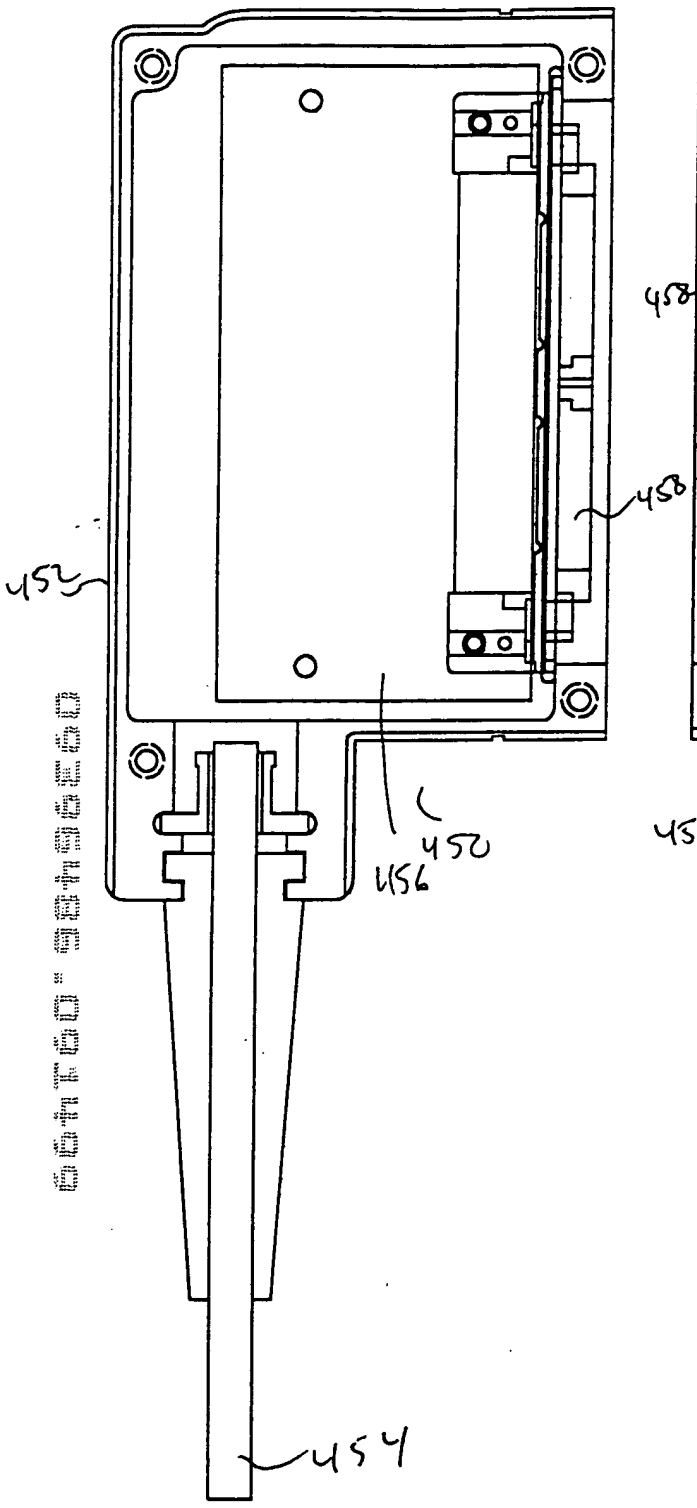


FIG 4I

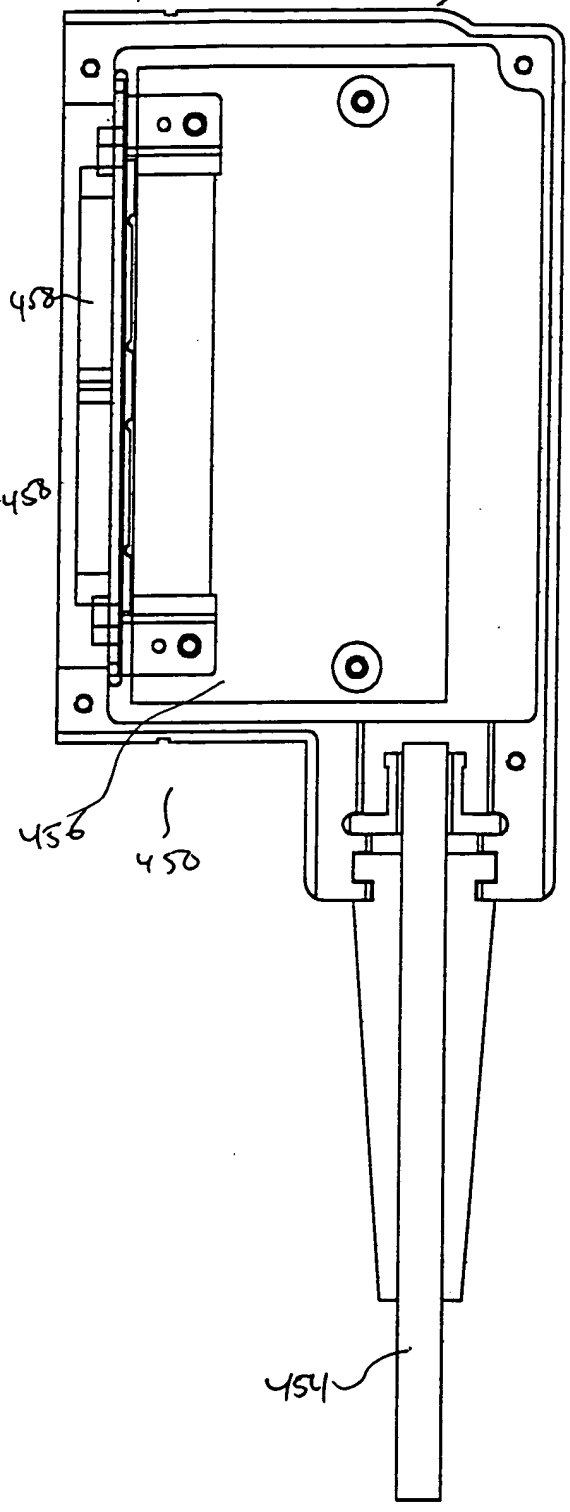
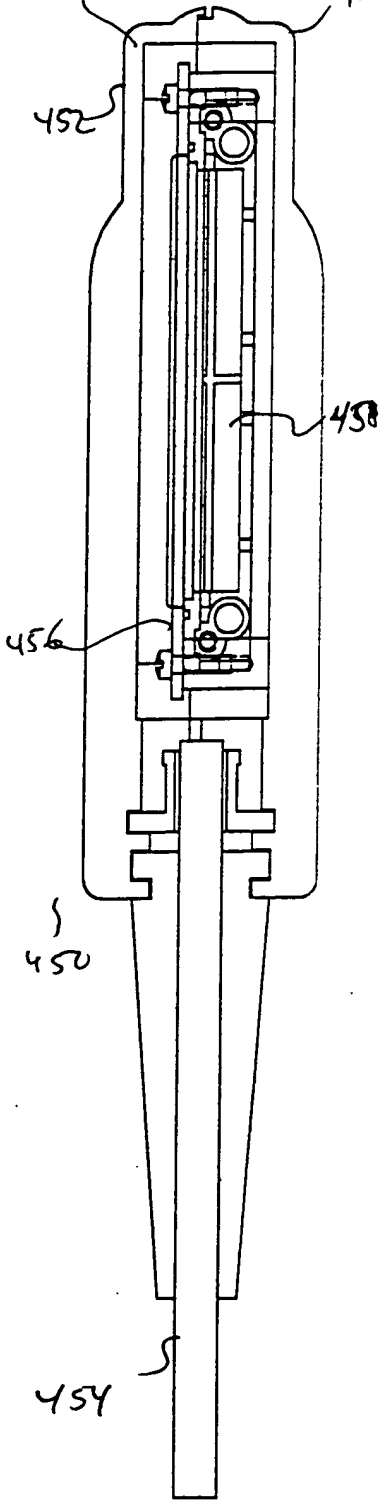


FIG 4J



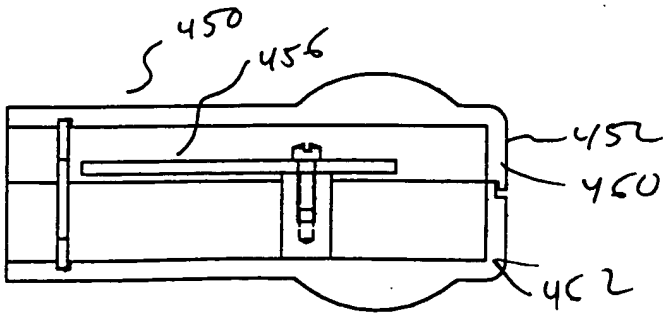


FIG 4K

Fig 4L

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
1	CHAN 1	41	BID_DATA	81	GROUND	121	TEMP_SENS
2	PRB_OUT 1	42	GROUND	82	CHAN 2	122	TEMP_RTN
3	CHAN 3	43	BID_CLOCK	83	GROUND	123	TEMP_REF
4	GROUND	44	GROUND	84	CHAN 4	124	GROUND
5	CHAN 5	45	!PID_WR	85	GROUND	125	PRB_PWR
6	GROUND	46	future use	86	CHAN 6	126	future use
7	CHAN 7	47	future use	87	GROUND	127	future use
8	GROUND	48	GROUND	88	CHAN 8	128	future use
9	CHAN 9	49	CHAN 33	89	GROUND	129	GROUND
10	GROUND	50	GROUND	90	CHAN 10	130	CHAN 34
11	CHAN 11	51	CHAN 35	91	GROUND	131	GROUND
12	GROUND	52	GROUND	92	CHAN 12	132	CHAN 36
13	CHAN 13	53	CHAN 37	93	GROUND	133	GROUND
14	GROUND	54	GROUND	94	CHAN 14	134	CHAN 38
15	CHAN 15	55	CHAN 39	95	GROUND	135	GROUND
16	GROUND	56	GROUND	96	CHAN 16	136	CHAN 40
17	CHAN 17	57	CHAN 41	97	GROUND	137	GROUND
18	GROUND	58	GROUND	98	CHAN 18	138	CHAN 42
19	CHAN 19	59	CHAN 43	99	GROUND	139	GROUND
20	GROUND	60	GROUND	100	CHAN 20	140	CHAN 44
21	CHAN 21	61	CHAN 45	101	GROUND	141	GROUND
22	GROUND	62	GROUND	102	CHAN 22	142	CHAN 46
23	CHAN 23	63	CHAN 47	103	GROUND	143	GROUND
24	GROUND	64	GROUND	104	CHAN 24	144	CHAN 48
25	CHAN 25	65	CHAN 49	105	GROUND	145	GROUND
26	GROUND	66	GROUND	106	CHAN 26	146	CHAN 50
27	CHAN 27	67	CHAN 51	107	GROUND	147	GROUND
28	GROUND	68	GROUND	108	CHAN 28	148	CHAN 52
29	CHAN 29	69	CHAN 53	109	GROUND	149	GROUND
30	GROUND	70	GROUND	110	CHAN 30	150	CHAN 54
31	CHAN 31	71	CHAN 55	111	GROUND	151	GROUND
32	GROUND	72	GROUND	112	CHAN 32	152	CHAN 56
33	future use	73	CHAN 57	113	GROUND	153	GROUND
34	future use	74	GROUND	114	future use	154	CHAN 58
35	future use	75	CHAN 59	115	future use	155	GROUND
36	future use	76	GROUND	116	GROUND	156	CHAN 60
37	future use	77	CHAN 61	117	UNUSED	157	GROUND
38	P_MUX_DAT	78	GROUND	118	SW_HV-	158	CHAN 62
39	P_MUX_CK	79	CHAN 63	119	UNUSED	159	PRB_OUT 2
40	P_MUX_ST	80	GROUND	120	SW_HV+	160	CHAN 64

2005-0000-00 Rev C

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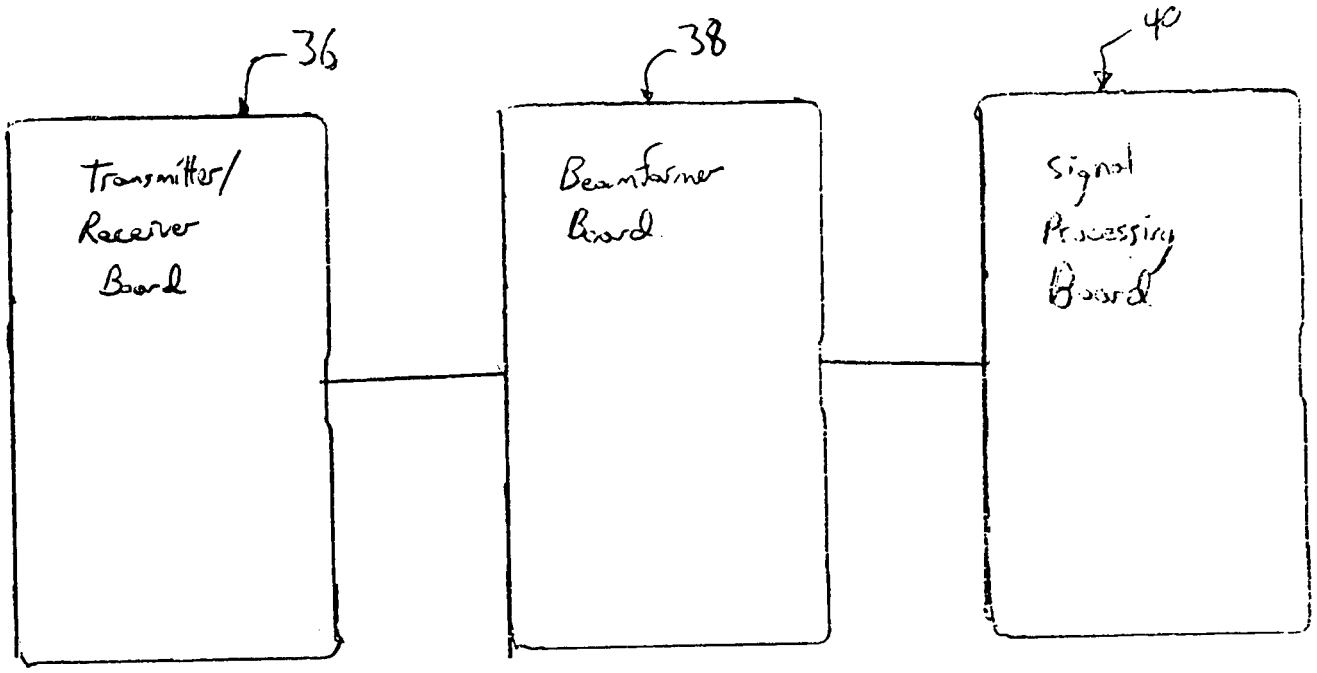

36
38
40
Transmitter/
Receiver
Board
Beamformer
Board
Signal
Processing
Board

Figure 5

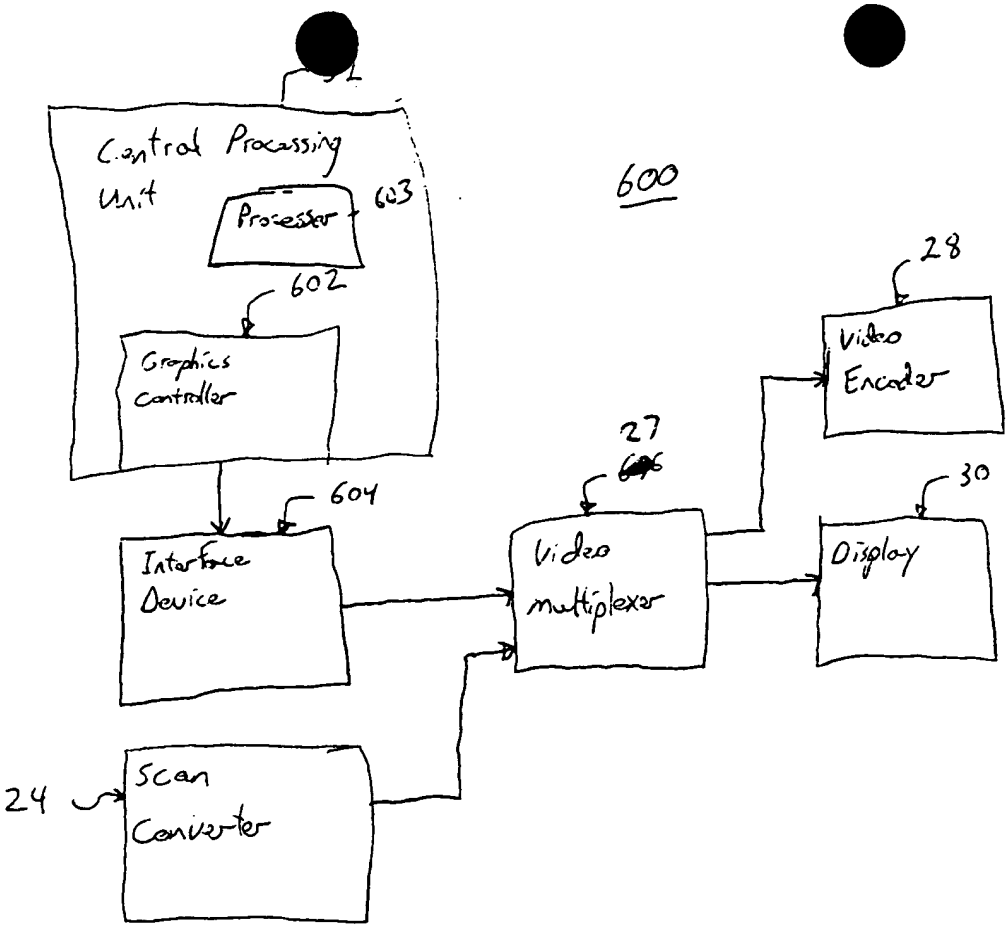

Central Processing Unit
Processor
603
602
Graphics controller
600
28
Video Encoder
27
604
30
Interface Device
Video multiplexer
Display
24
Scan Converter

FIG. 6

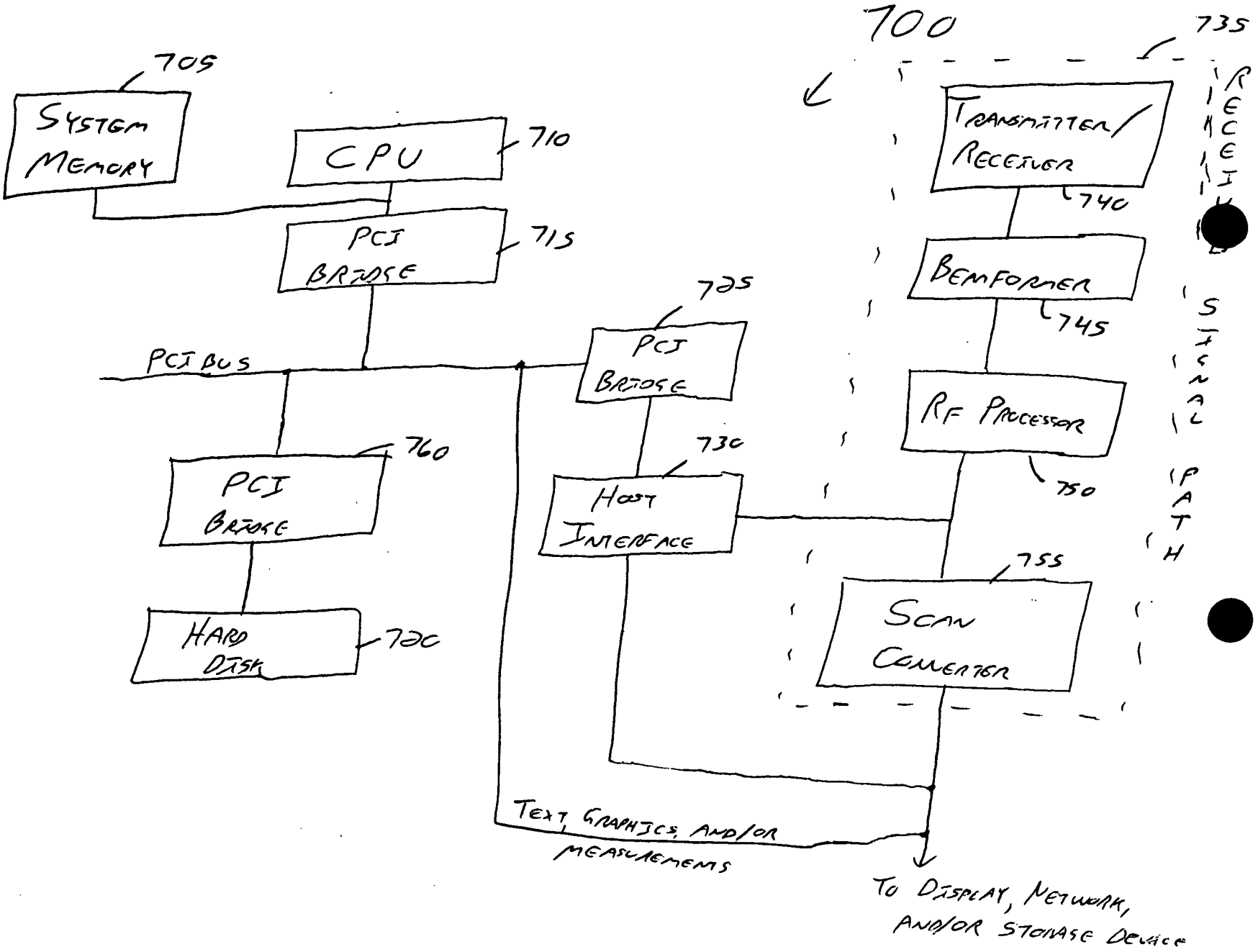

700
735
705
SYSTEM MEMORY
CPU
710
PCI BRIDGE
715
725
PCI BRIDGE
PCI BUS
760
PCI BRIDGE
730
HOST INTERFACE
HARD DISK
720
TRANSMITTER/ RECEIVER
740
BEAMFORMER
745
RF PROCESSOR
750
SCAN CONVERTER
755
RECEIVE SIGNAL PATH
TEXT, GRAPHICS, AND/OR MEASUREMENTS
TO DISPLAY, NETWORK, AND/OR STORAGE DEVICE

FIGURE 7

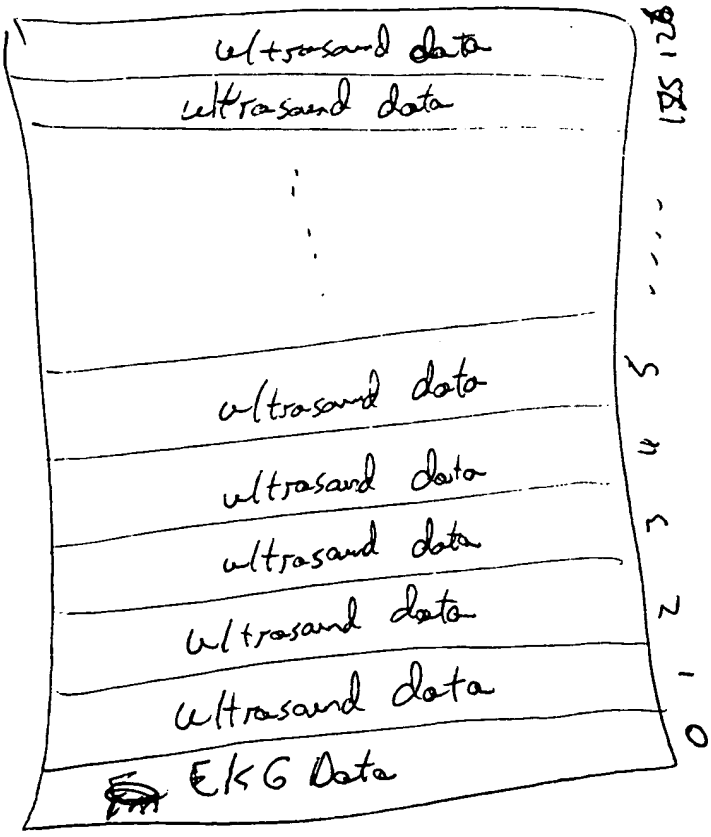

ultrasound data
ultrasound data
ultrasound data
ultrasound data
ultrasound data
ultrasound data
EKG Data
128
1
2
3
4
5
n

FIG. 8

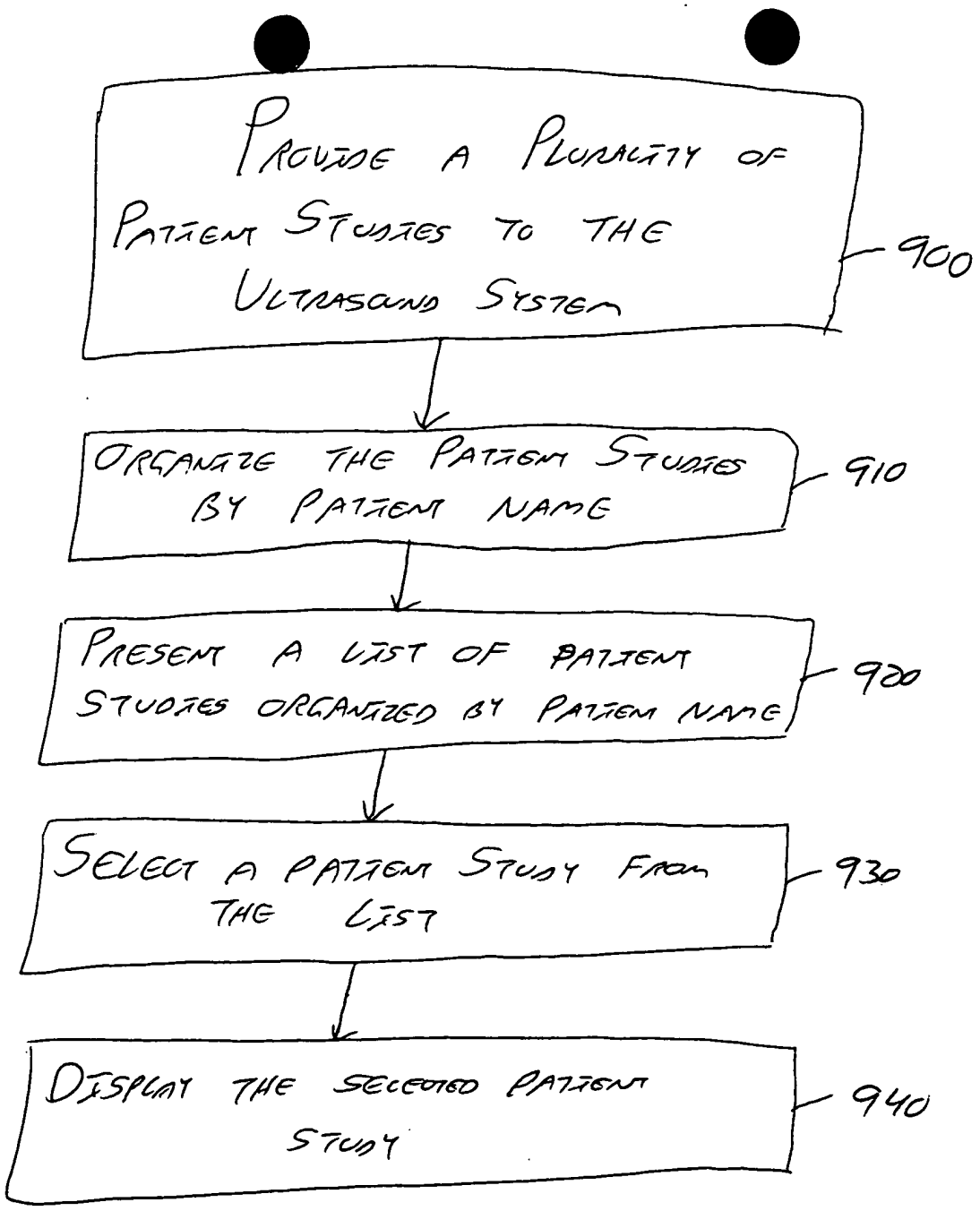

PROVIDE A PLURALITY OF PATIENT STUDIES TO THE ULTRASOUND SYSTEM
900
ORGANIZE THE PATIENT STUDIES BY PATIENT NAME
910
PRESENT A LIST OF PATIENT STUDIES ORGANIZED BY PATIENT NAME
920
SELECT A PATIENT STUDY FROM THE LIST
930
DISPLAY THE SELECTED PATIENT STUDY
940

FIGURE 9

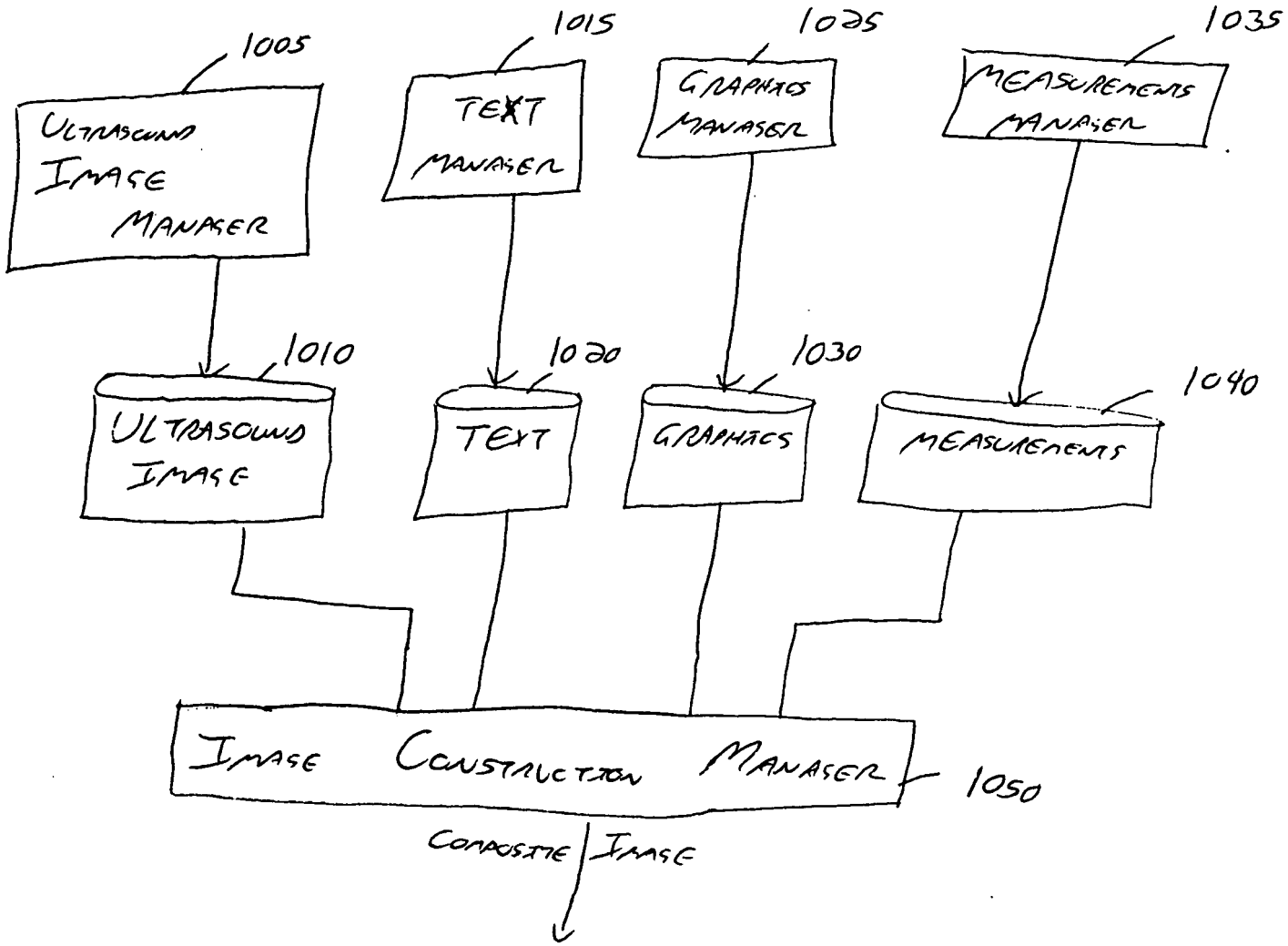

1005
ULTRASOUND IMAGE MANAGER
1015
TEXT MANAGER
1025
GRAPHICS MANAGER
1035
MEASUREMENTS MANAGER
1010
ULTRASOUND IMAGE
1020
TEXT
1030
GRAPHICS
1040
MEASUREMENTS
IMAGE CONSTRUCTION MANAGER
1050
COMPOSITE IMAGE

FIGURE 10

Getty Images

200

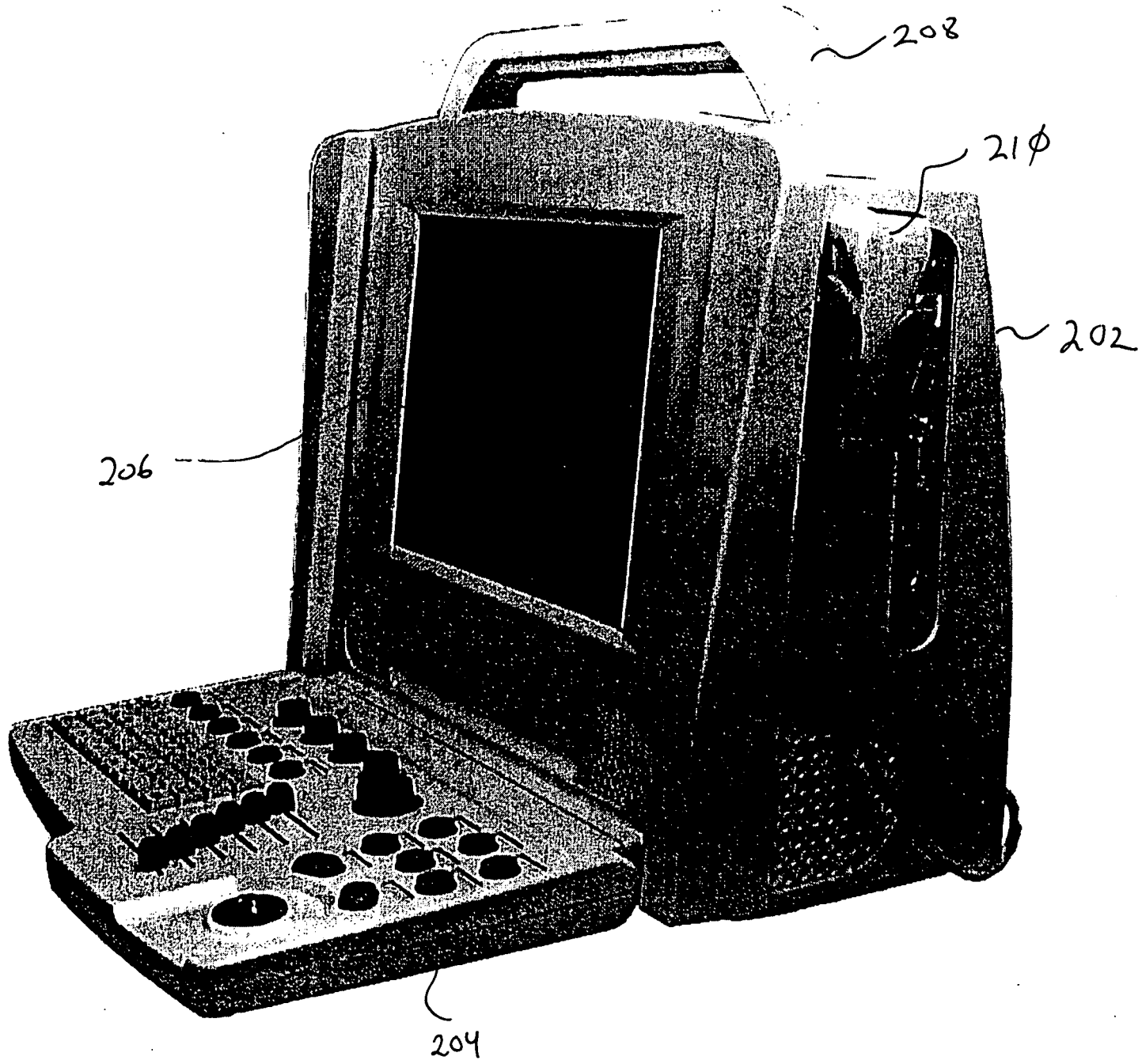


FIG 11

66hT60" 98h96E60

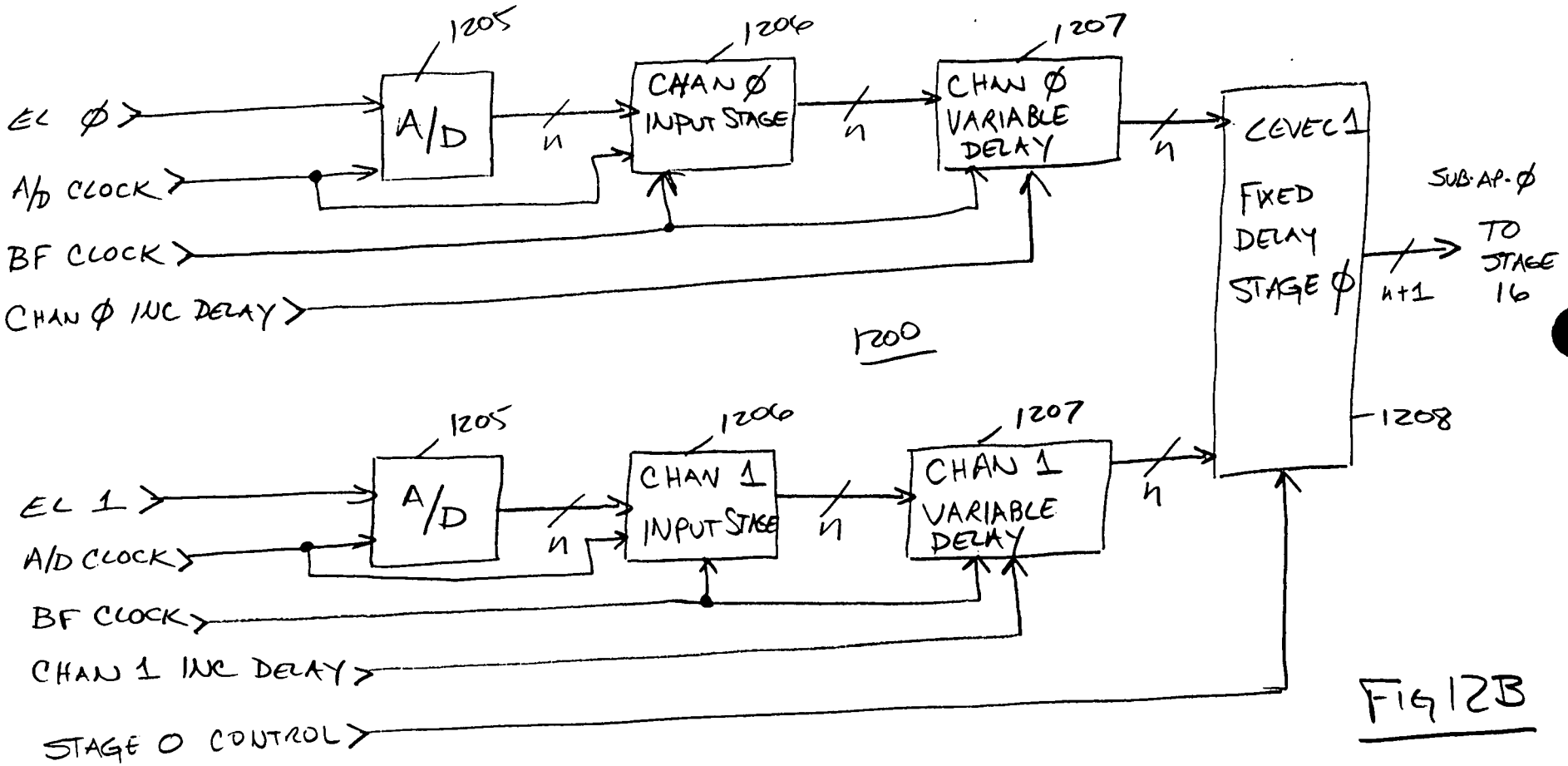


Fig 12B

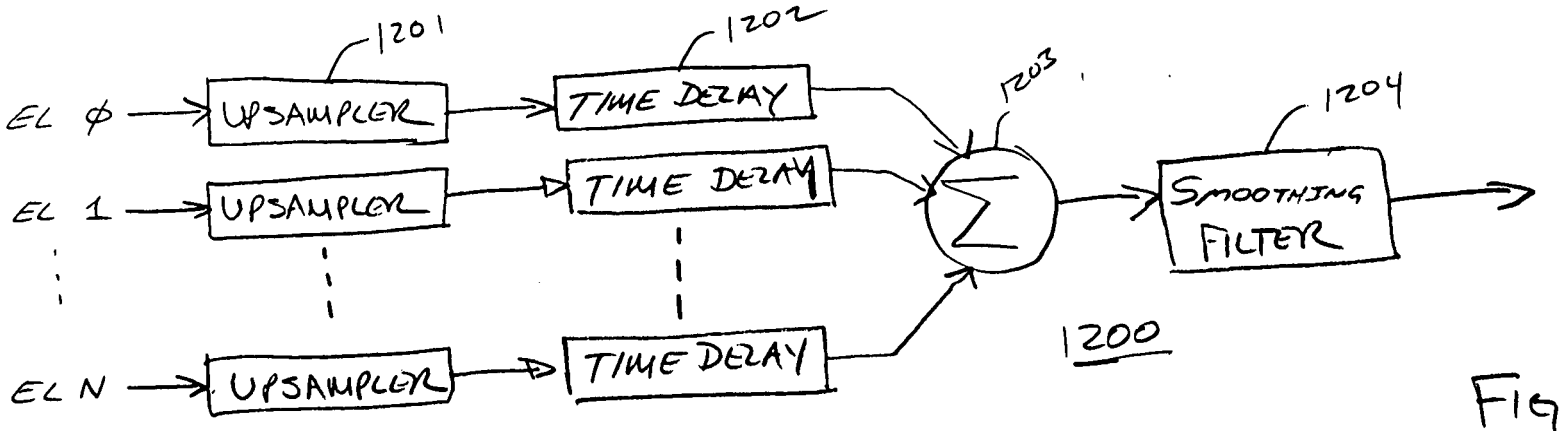


Fig 12A

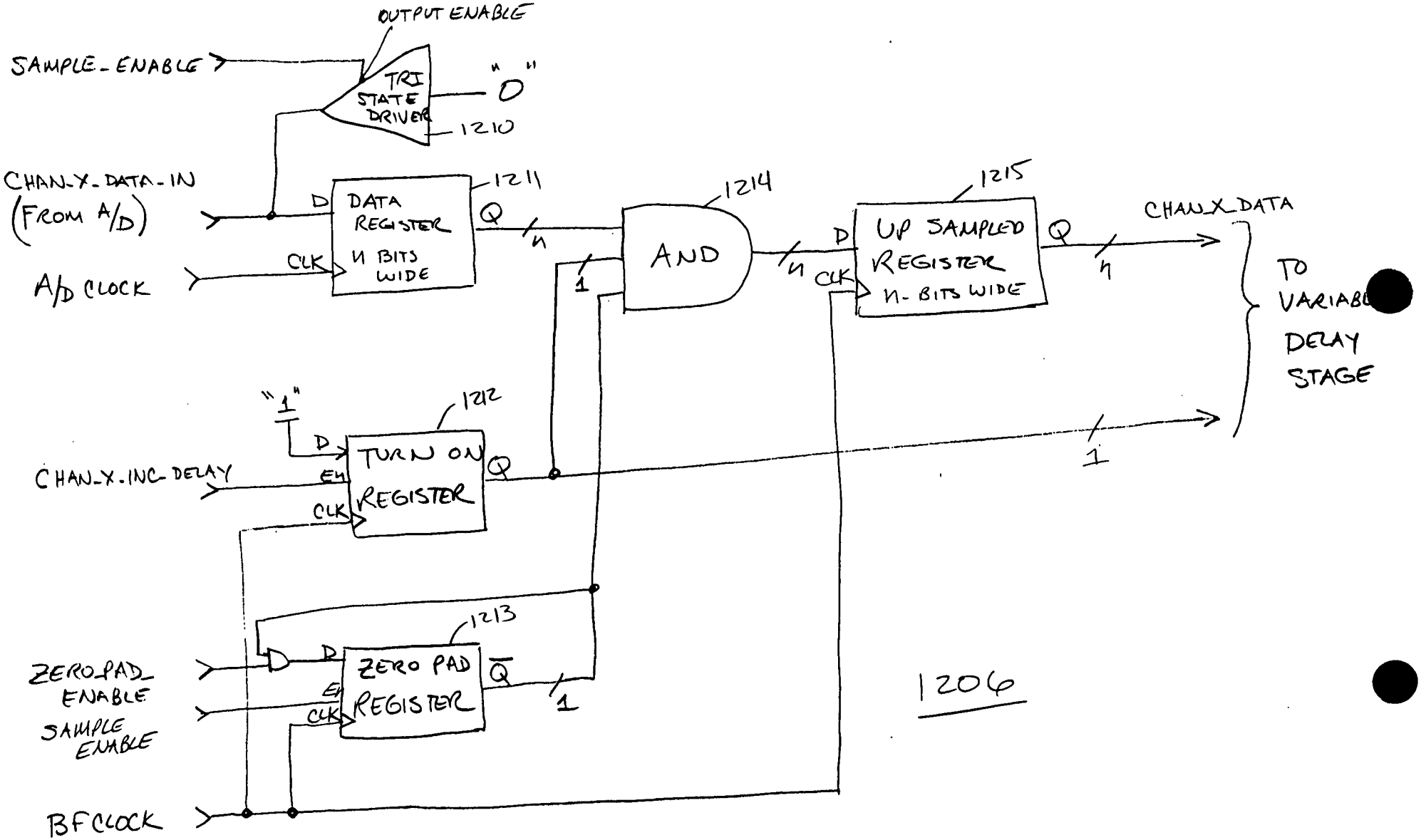

OUTPUT ENABLE
SAMPLE_ENABLE
TRI STATE DRIVER
"0"
1210
CHAN_X_DATA_IN (FROM A/D)
D
DATA REGISTER
N BITS WIDE
CLK
Q
1211
A/D CLOCK
1214
AND
1
1215
UP SAMPLED REGISTER
N-BITS WIDE
CHAN_X_DATA
TO VARIABLE DELAY STAGE
"1"
1212
TURN ON REGISTER
CHAN_X_INC_DELAY
EN
1213
ZERO PAD REGISTER
ZERO_PAD_ENABLE
SAMPLE ENABLE
BFCLOCK
1206

Fig 12C

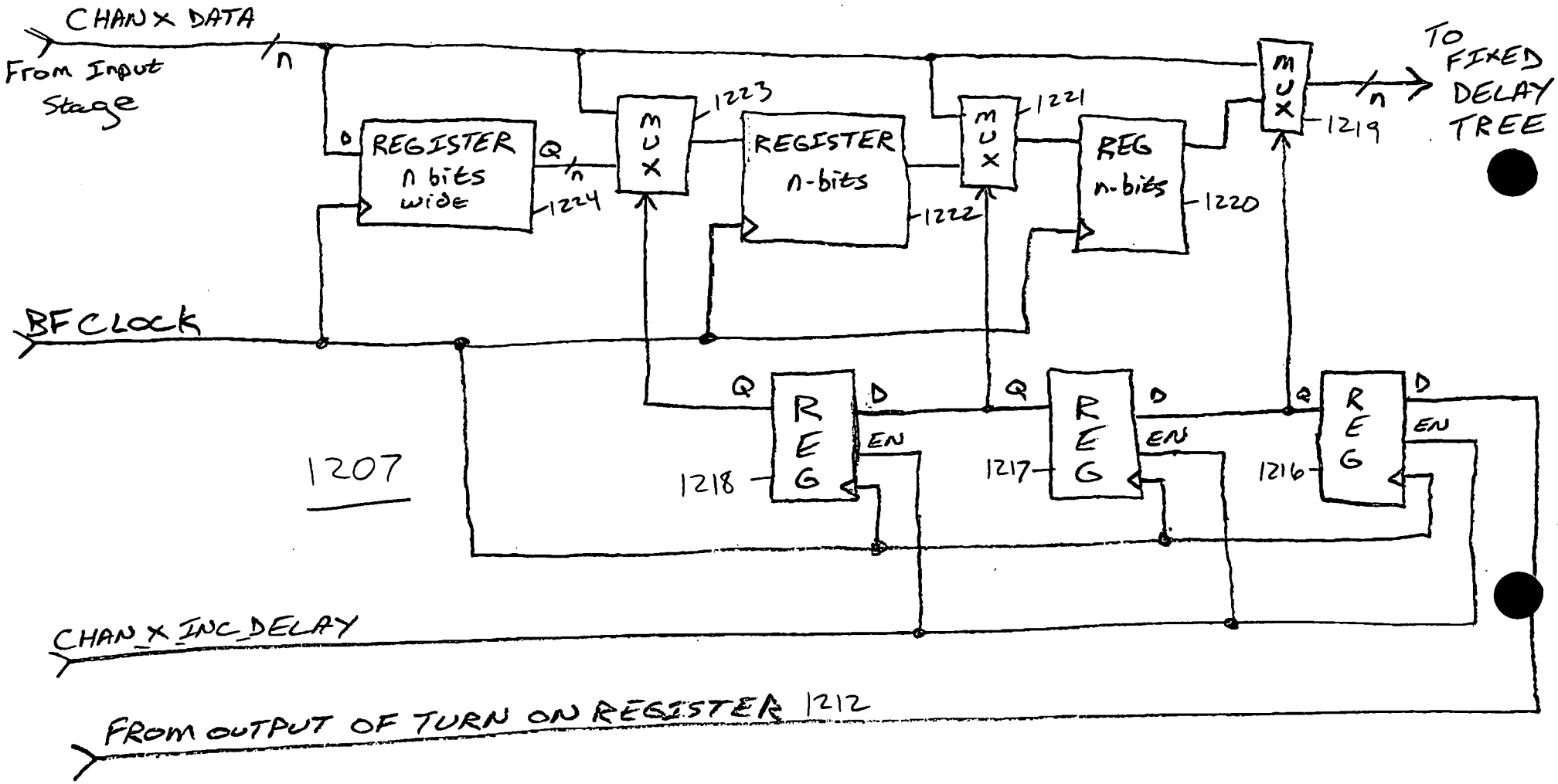

CHAN X DATA
From Input Stage
n
REGISTER n bits wide
D
Q
n
1224
MUX
1223
REGISTER n-bits
1222
MUX
1221
REG n-bits
1220
MUX
1219
n
TO FIXED DELAY TREE
BF CLOCK
1207
Q
D
EN
REG
1218
Q
D
EN
REG
1217
Q
D
EN
REG
1216
CHAN_X_INC_DELAY
FROM OUTPUT OF TURN ON REGISTER 1212

FIG 12D

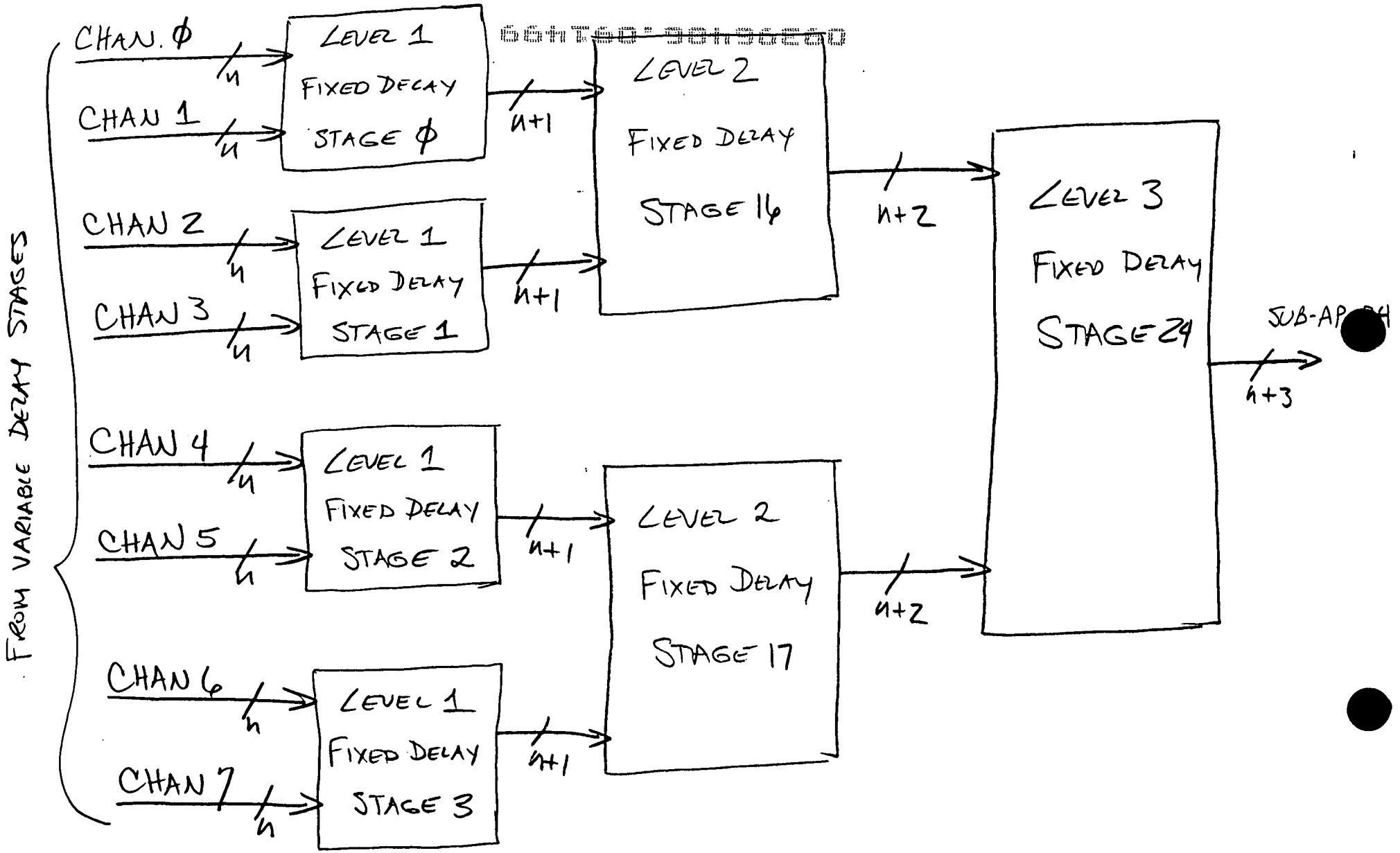

FROM VARIABLE DELAY STAGES
CHAN. ϕ
CHAN 1
CHAN 2
CHAN 3
CHAN 4
CHAN 5
CHAN 6
CHAN 7
n
LEVEL 1 FIXED DELAY STAGE ϕ
LEVEL 1 FIXED DELAY STAGE 1
LEVEL 1 FIXED DELAY STAGE 2
LEVEL 1 FIXED DELAY STAGE 3
n+1
LEVEL 2 FIXED DELAY STAGE 16
LEVEL 2 FIXED DELAY STAGE 17
n+2
LEVEL 3 FIXED DELAY STAGE 24
SUB-AP
n+3

FIG 12E

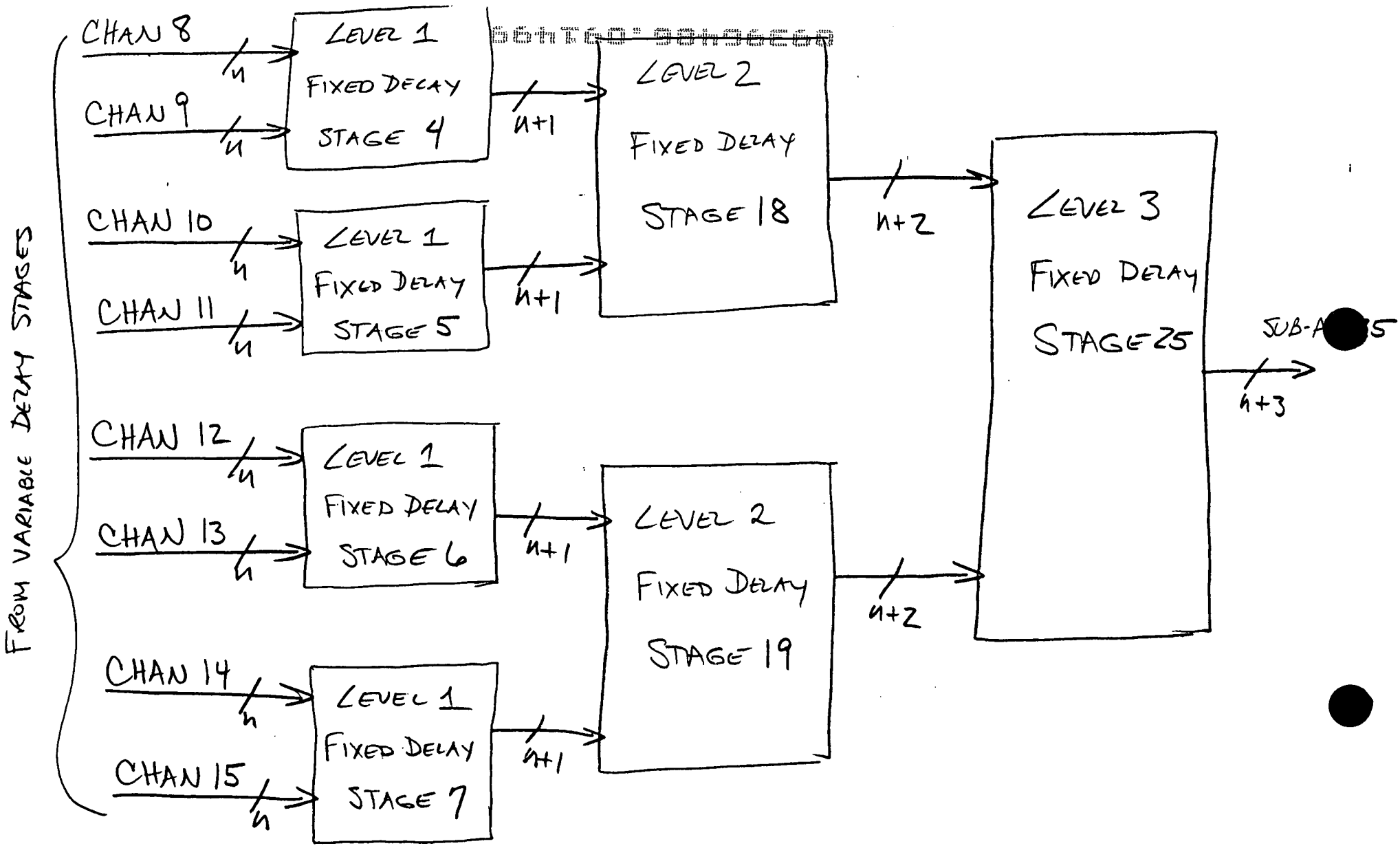

FROM VARIABLE DELAY STAGES
CHAN 8
CHAN 9
CHAN 10
CHAN 11
CHAN 12
CHAN 13
CHAN 14
CHAN 15
n
LEVEL 1 FIXED DELAY STAGE 4
LEVEL 1 FIXED DELAY STAGE 5
LEVEL 1 FIXED DELAY STAGE 6
LEVEL 1 FIXED DELAY STAGE 7
n+1
LEVEL 2 FIXED DELAY STAGE 18
LEVEL 2 FIXED DELAY STAGE 19
n+2
LEVEL 3 FIXED DELAY STAGE 25
n+3
SUB-A 5

Fig 12F

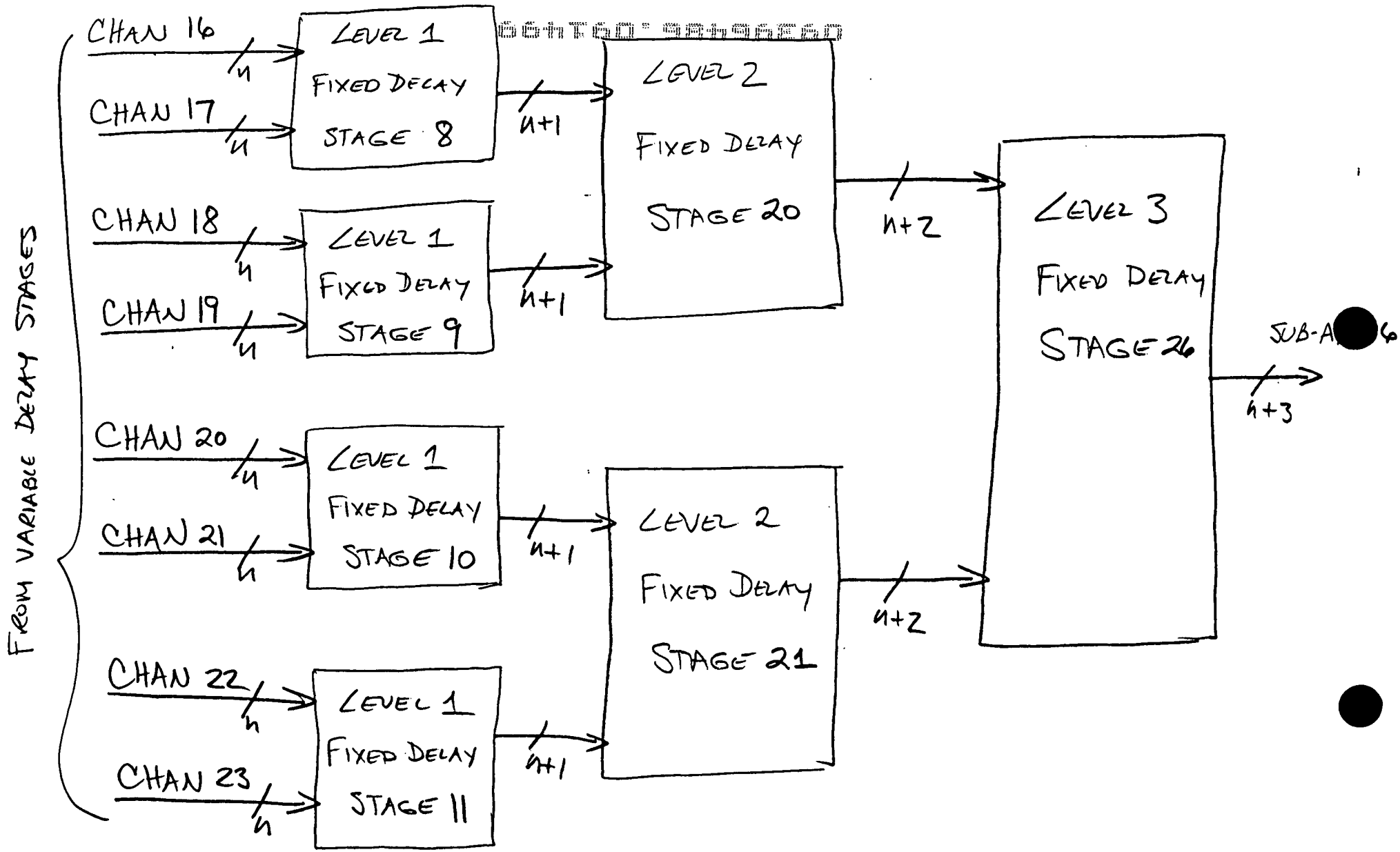

FROM VARIABLE DELAY STAGES
CHAN 16
CHAN 17
CHAN 18
CHAN 19
CHAN 20
CHAN 21
CHAN 22
CHAN 23
n
LEVEL 1
FIXED DELAY
STAGE 8
LEVEL 1
FIXED DELAY
STAGE 9
LEVEL 1
FIXED DELAY
STAGE 10
LEVEL 1
FIXED DELAY
STAGE 11
n+1
LEVEL 2
FIXED DELAY
STAGE 20
LEVEL 2
FIXED DELAY
STAGE 21
n+2
LEVEL 3
FIXED DELAY
STAGE 26
n+3
SUB-A

Fig 12G

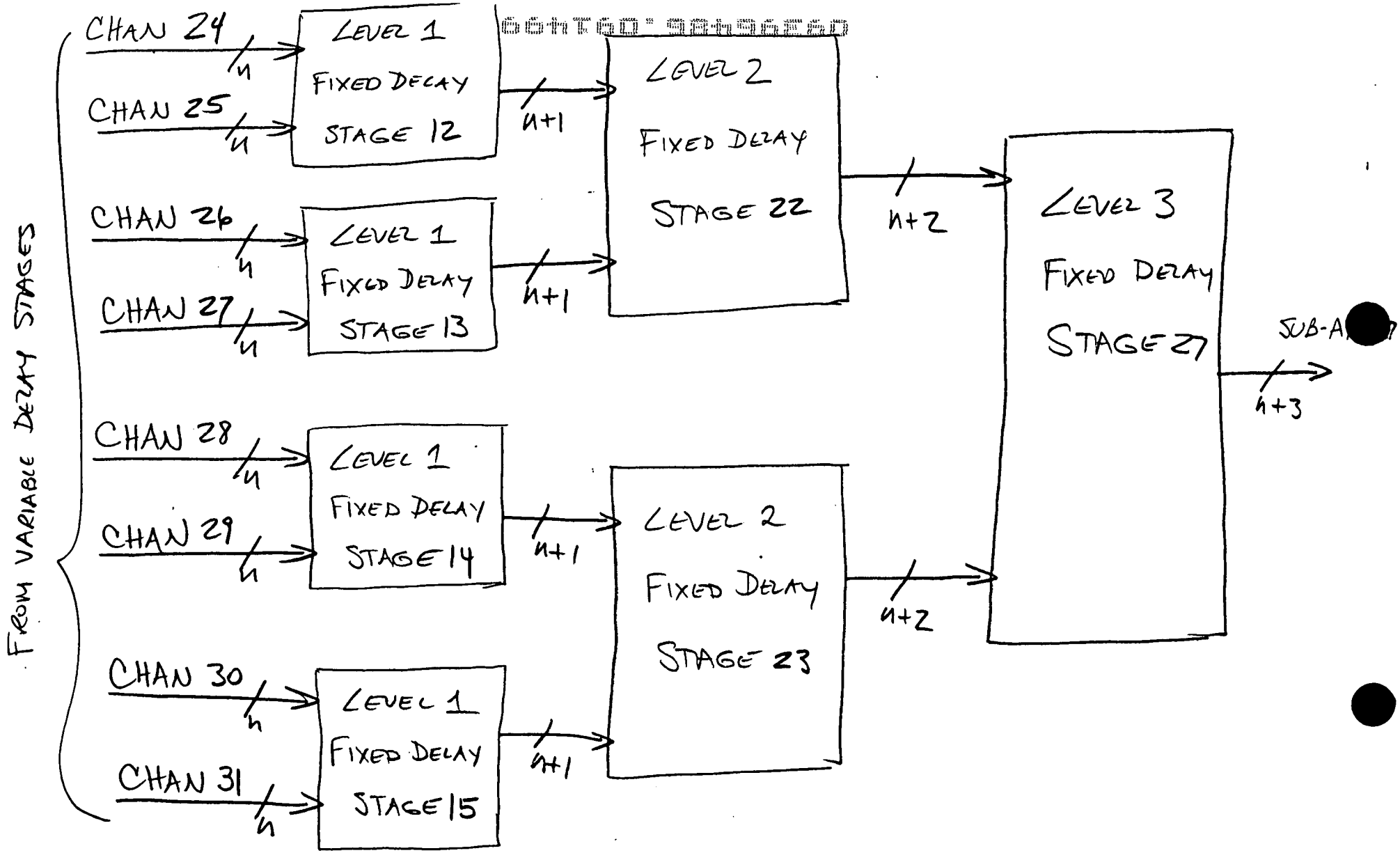

FROM VARIABLE DELAY STAGES
CHAN 24
CHAN 25
CHAN 26
CHAN 27
CHAN 28
CHAN 29
CHAN 30
CHAN 31
n
LEVEL 1
FIXED DELAY
STAGE 12
STAGE 13
STAGE 14
STAGE 15
n+1
LEVEL 2
FIXED DELAY
STAGE 22
STAGE 23
n+2
LEVEL 3
FIXED DELAY
STAGE 27
n+3

FIG 12H

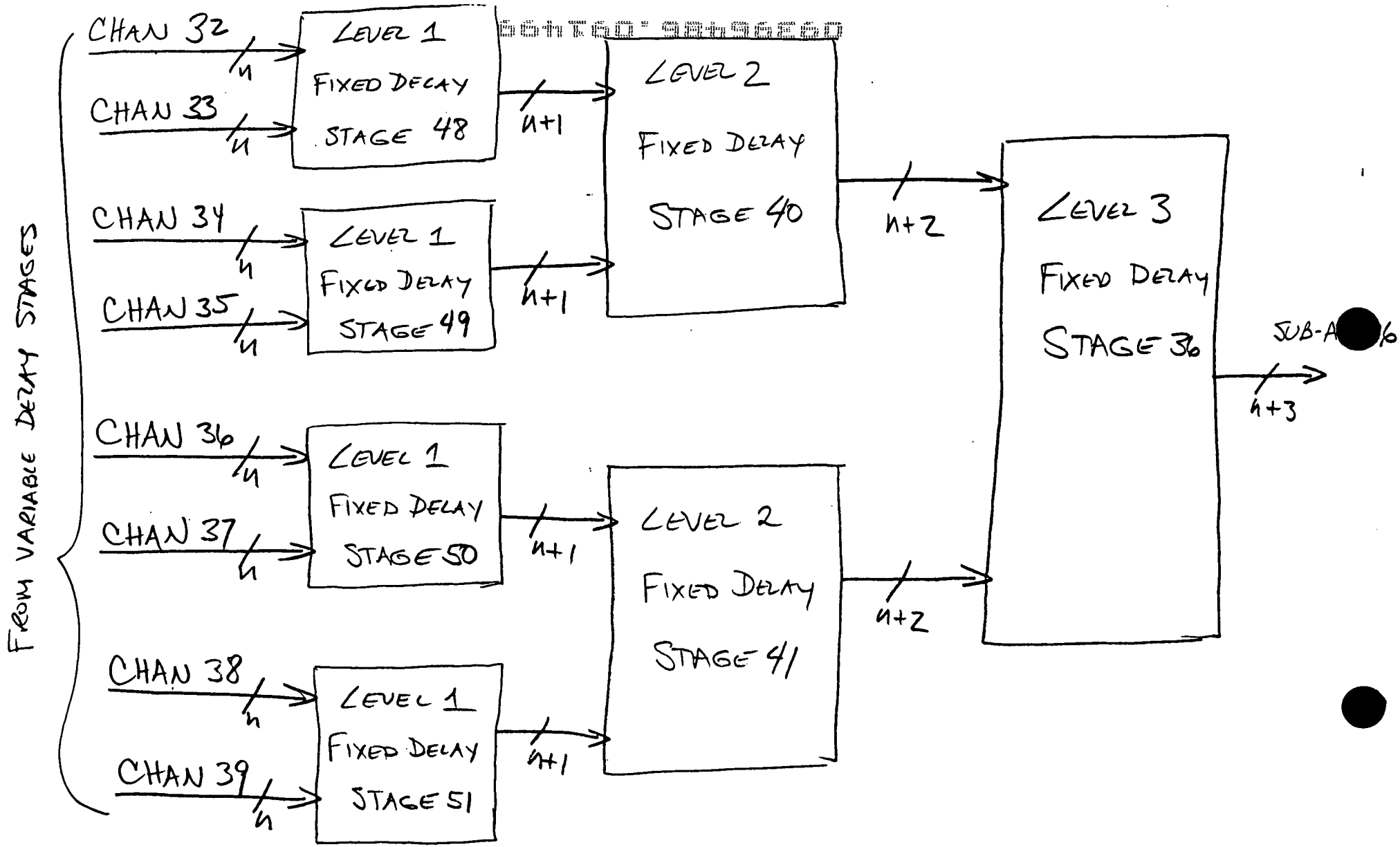

FROM VARIABLE DELAY STAGES
CHAN 32
CHAN 33
CHAN 34
CHAN 35
CHAN 36
CHAN 37
CHAN 38
CHAN 39
n
LEVEL 1
FIXED DELAY
STAGE 48
LEVEL 1
FIXED DELAY
STAGE 49
LEVEL 1
FIXED DELAY
STAGE 50
LEVEL 1
FIXED DELAY
STAGE 51
n+1
LEVEL 2
FIXED DELAY
STAGE 40
LEVEL 2
FIXED DELAY
STAGE 41
n+2
LEVEL 3
FIXED DELAY
STAGE 36
n+3
SUB-A

Fig 12I

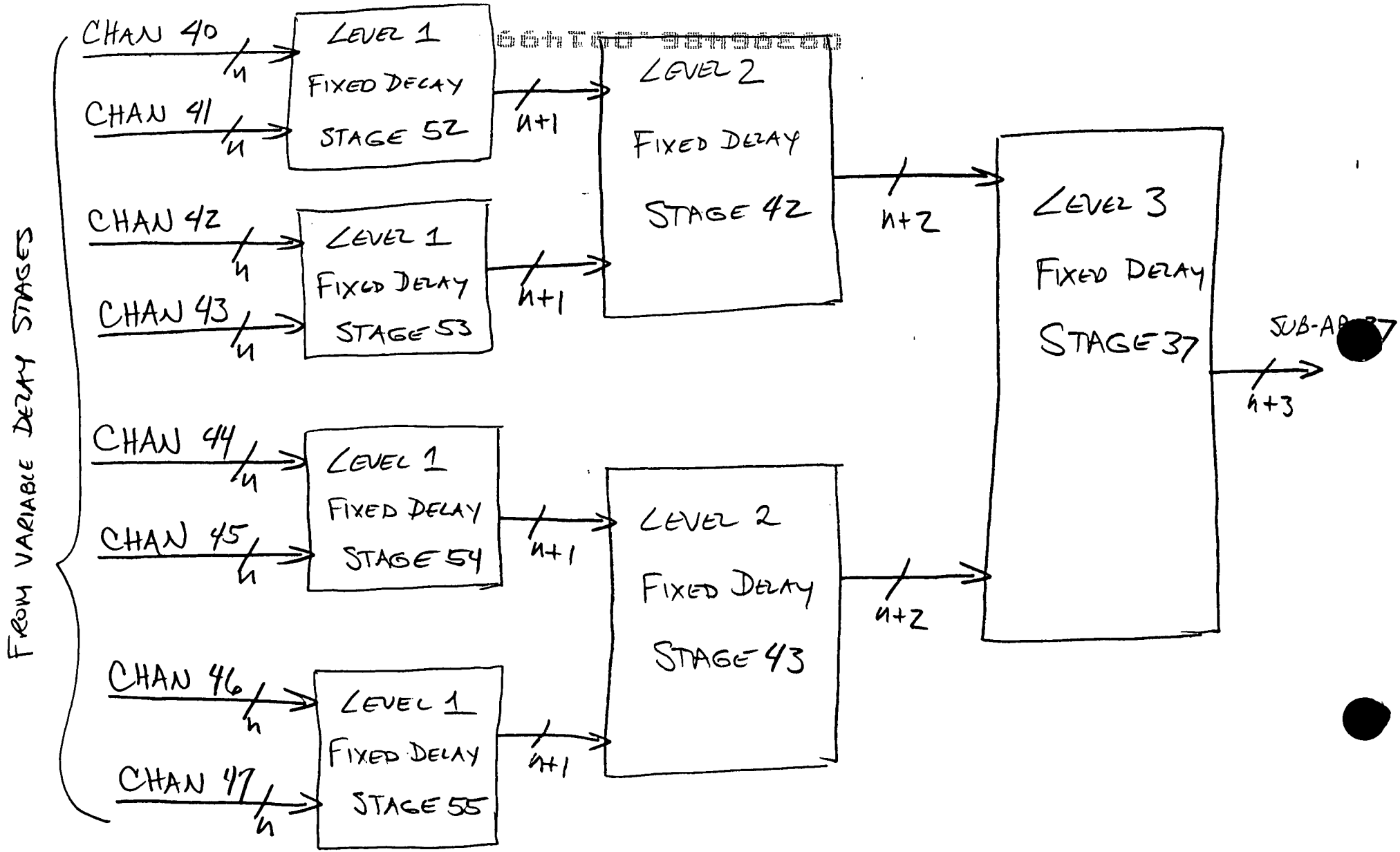

FROM VARIABLE DELAY STAGES
CHAN 40
CHAN 41
CHAN 42
CHAN 43
CHAN 44
CHAN 45
CHAN 46
CHAN 47
n
LEVEL 1 FIXED DELAY STAGE 52
LEVEL 1 FIXED DELAY STAGE 53
LEVEL 1 FIXED DELAY STAGE 54
LEVEL 1 FIXED DELAY STAGE 55
n+1
LEVEL 2 FIXED DELAY STAGE 42
LEVEL 2 FIXED DELAY STAGE 43
n+2
LEVEL 3 FIXED DELAY STAGE 37
n+3

Fig 12J

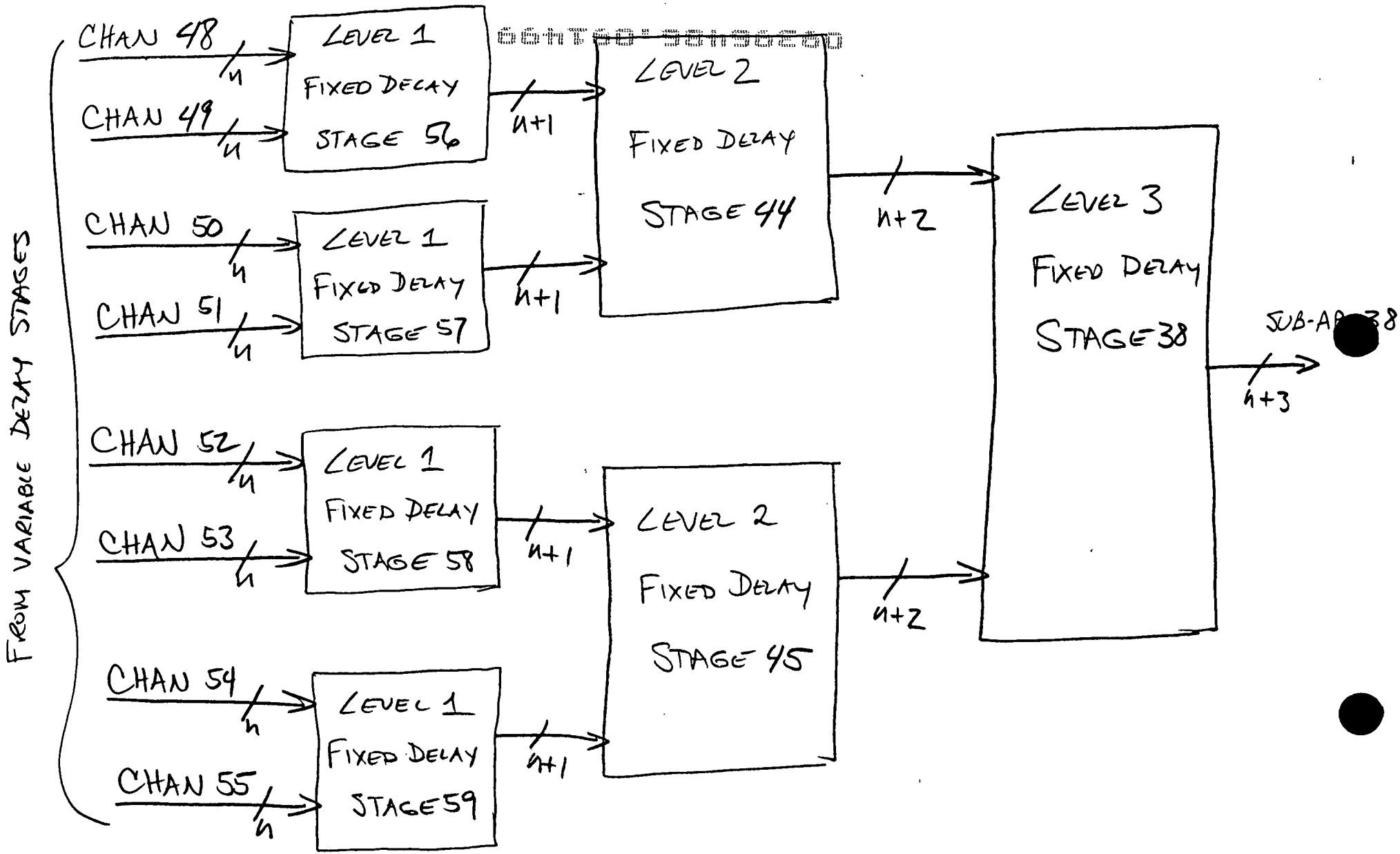

FROM VARIABLE DELAY STAGES
CHAN 48
CHAN 49
CHAN 50
CHAN 51
CHAN 52
CHAN 53
CHAN 54
CHAN 55
n
LEVEL 1 FIXED DELAY STAGE 56
LEVEL 1 FIXED DELAY STAGE 57
LEVEL 1 FIXED DELAY STAGE 58
LEVEL 1 FIXED DELAY STAGE 59
n+1
LEVEL 2 FIXED DELAY STAGE 44
LEVEL 2 FIXED DELAY STAGE 45
n+2
LEVEL 3 FIXED DELAY STAGE 38
n+3

Fig12K

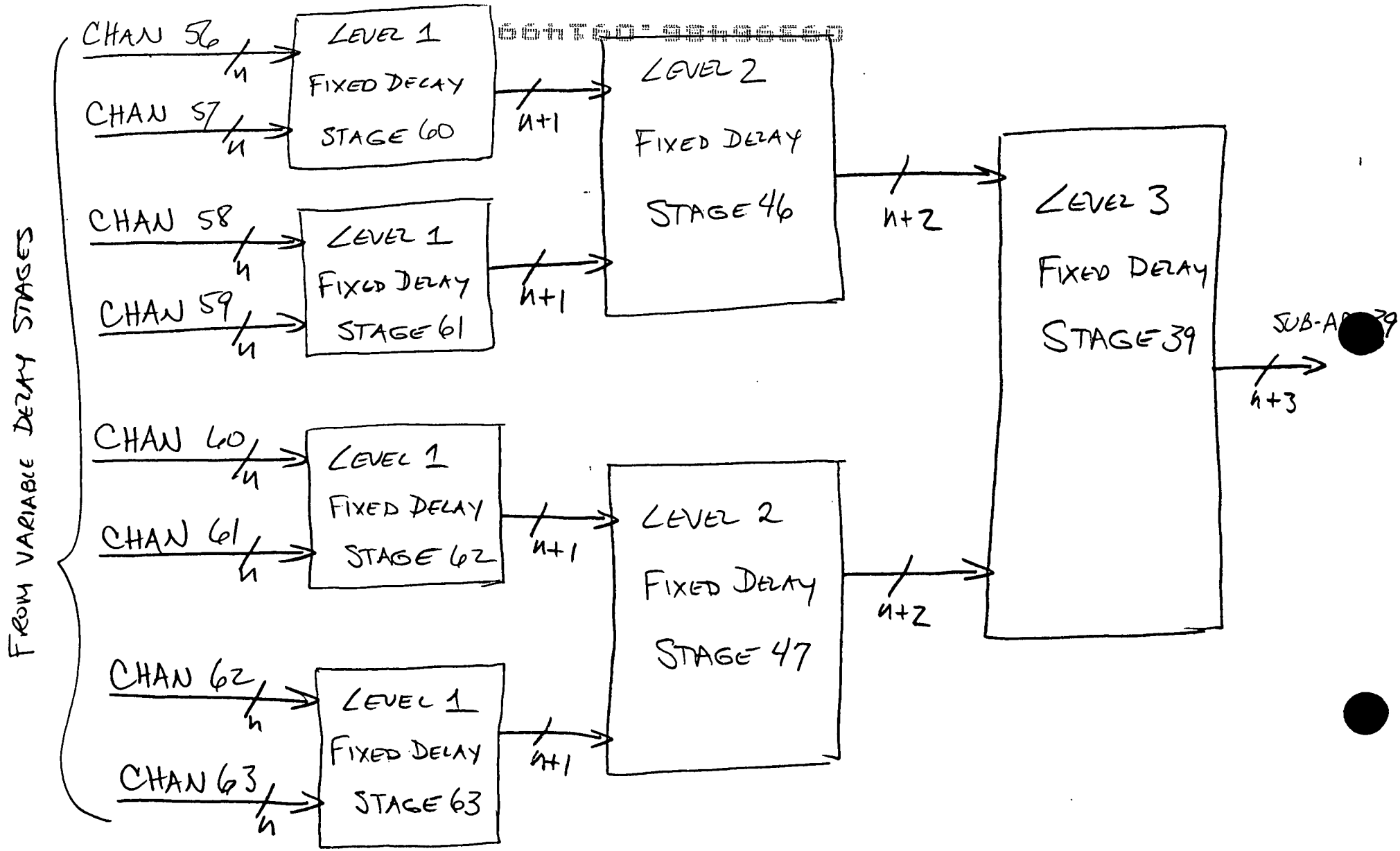

FROM VARIABLE DELAY STAGES
CHAN 56
CHAN 57
CHAN 58
CHAN 59
CHAN 60
CHAN 61
CHAN 62
CHAN 63
n
LEVEL 1 FIXED DELAY STAGE 60
LEVEL 1 FIXED DELAY STAGE 61
LEVEL 1 FIXED DELAY STAGE 62
LEVEL 1 FIXED DELAY STAGE 63
n+1
LEVEL 2 FIXED DELAY STAGE 46
LEVEL 2 FIXED DELAY STAGE 47
n+2
LEVEL 3 FIXED DELAY STAGE 39
n+3

FIG 12L

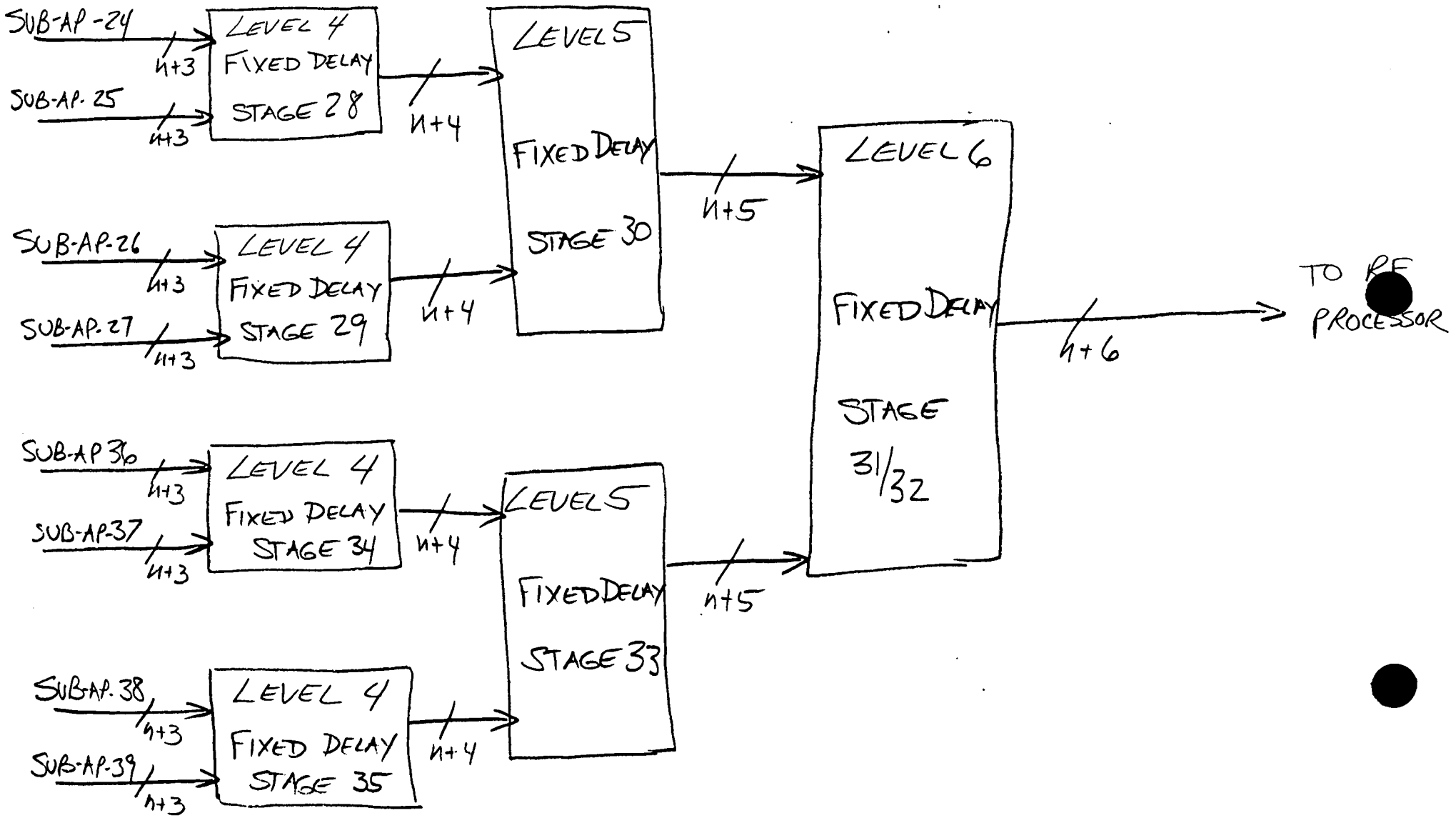

SUB-AP-24
SUB-AP-25
n+3
n+3
LEVEL 4
FIXED DELAY
STAGE 28
n+4
LEVEL 5
FIXED DELAY
STAGE 30
SUB-AP-26
SUB-AP-27
n+3
n+3
LEVEL 4
FIXED DELAY
STAGE 29
n+4
n+5
LEVEL 6
FIXED DELAY
STAGE
31/32
n+6
TO RF
PROCESSOR
SUB-AP 36
SUB-AP-37
n+3
n+3
LEVEL 4
FIXED DELAY
STAGE 34
n+4
LEVEL 5
FIXED DELAY
STAGE 33
n+5
SUB-AP. 38
SUB-AP-39
n+3
n+3
LEVEL 4
FIXED DELAY
STAGE 35
n+4

Fig 12M

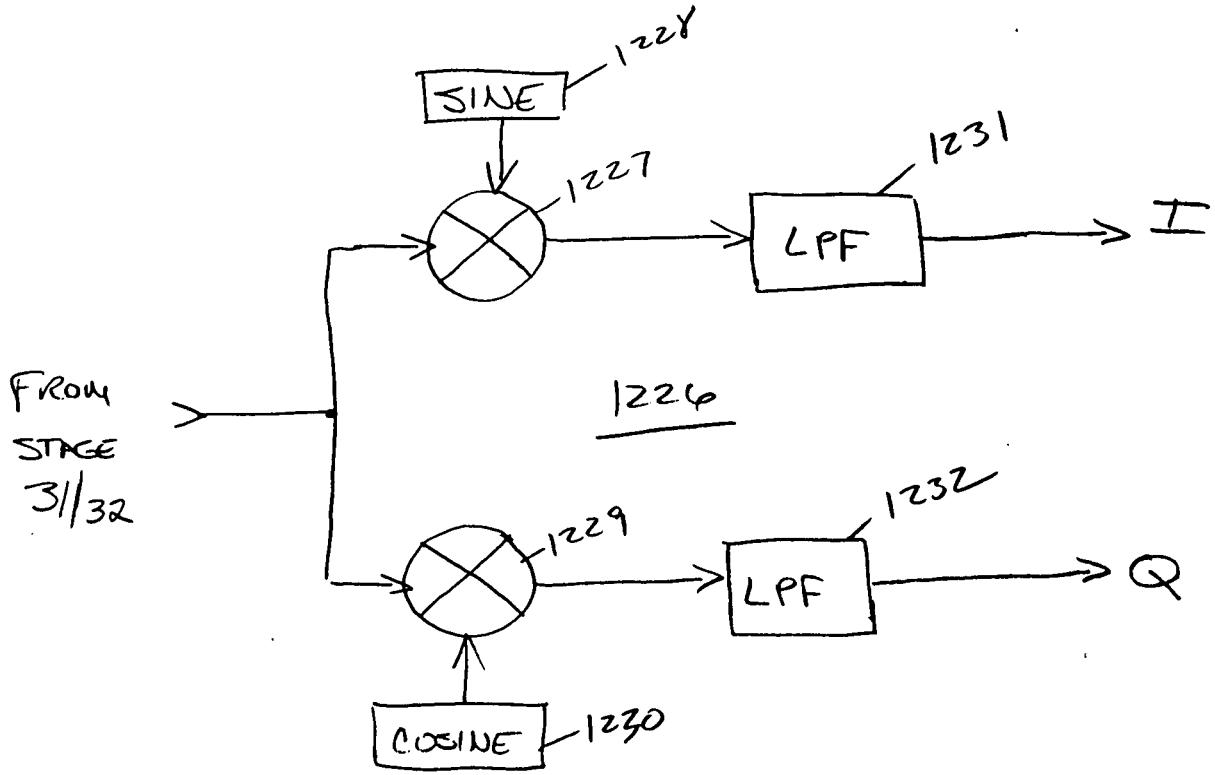


FIG 12N

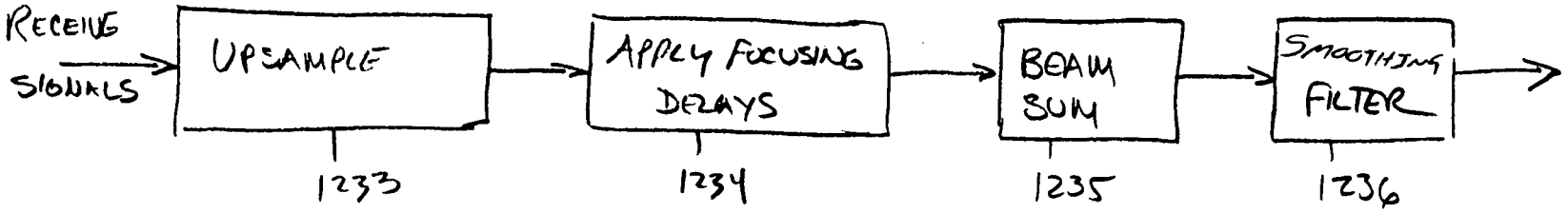


FIG 12O

6,175,849 B1

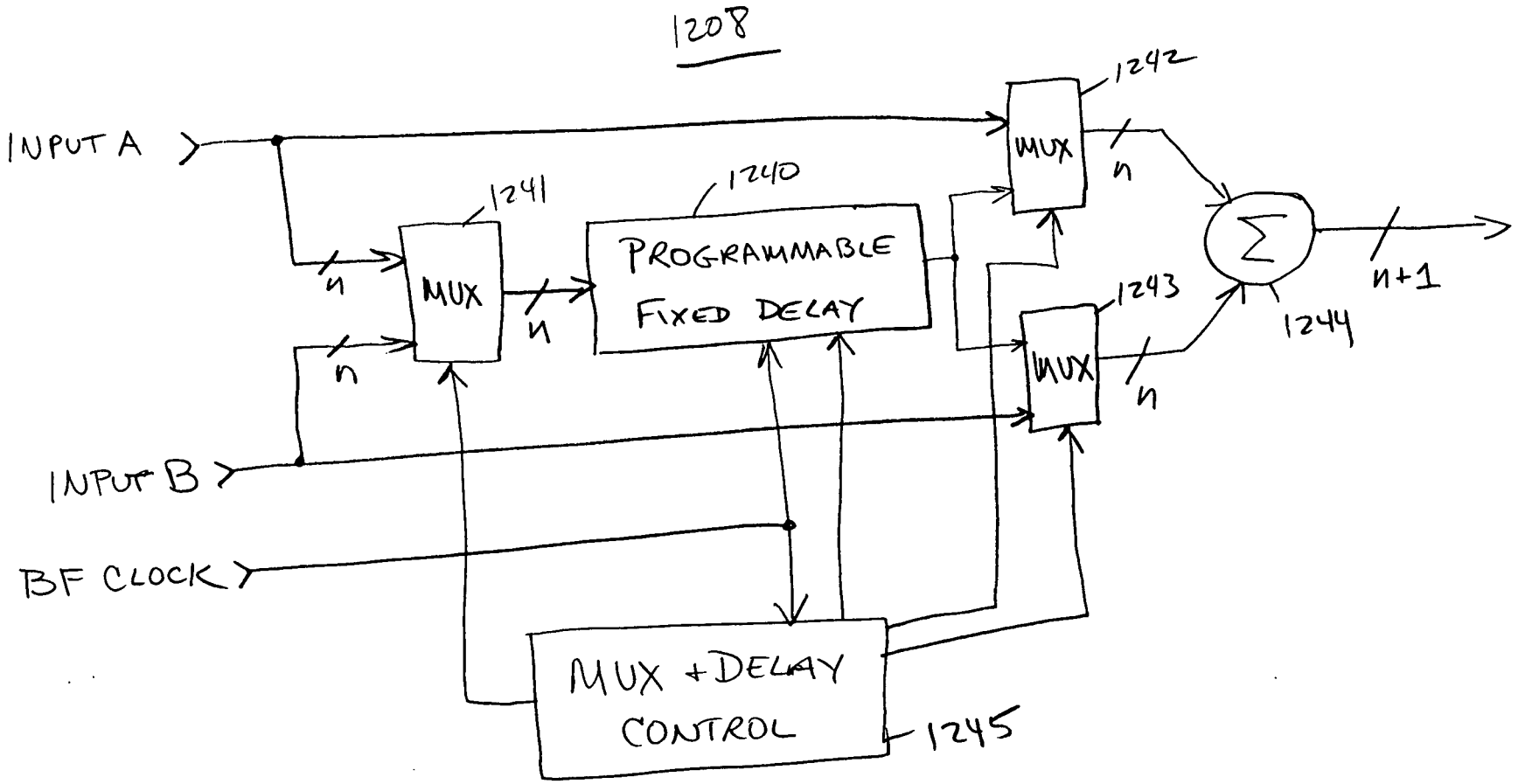


FIG 12P

6,116,760 - 9/19/2000

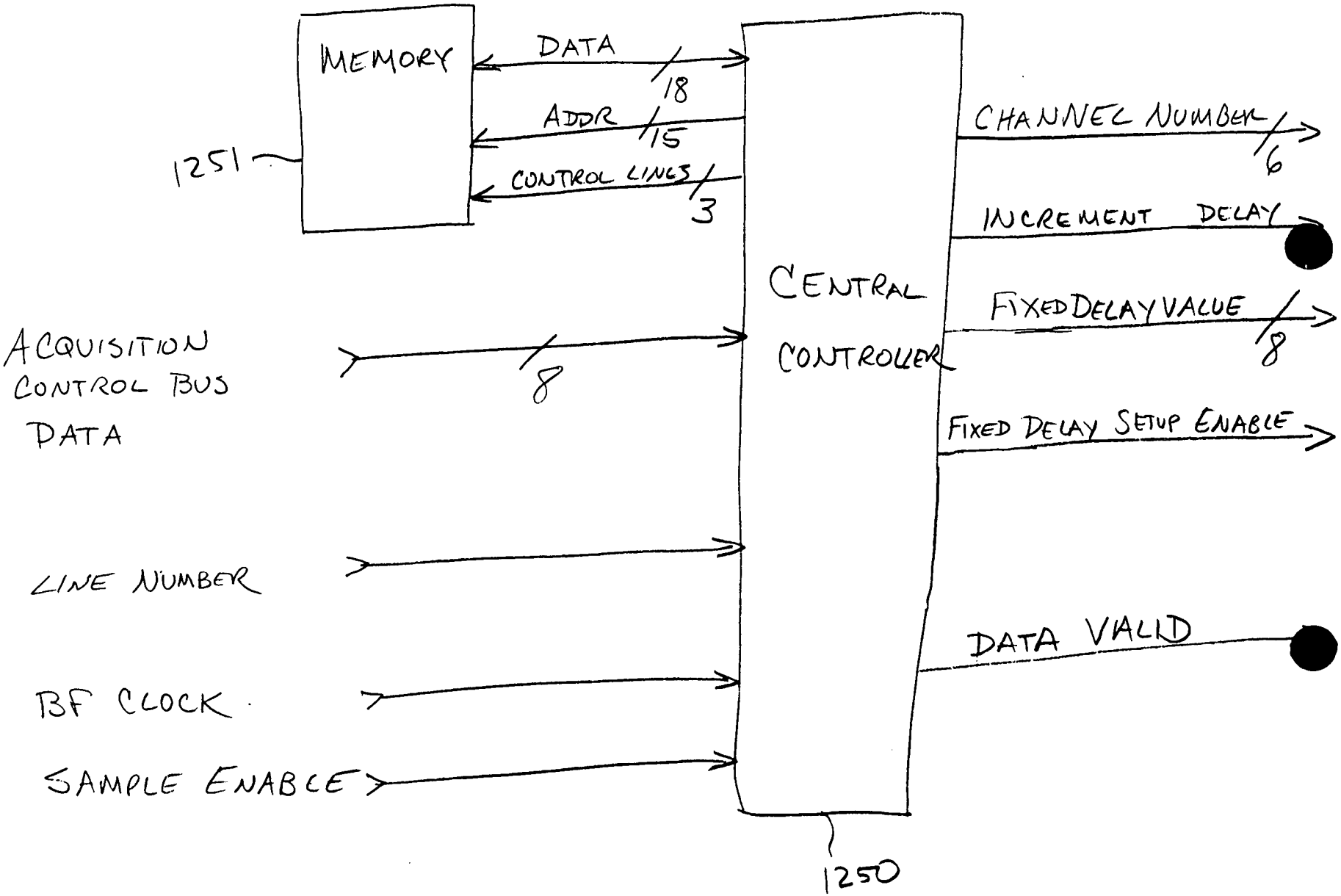


Fig 12Q

6,870,961

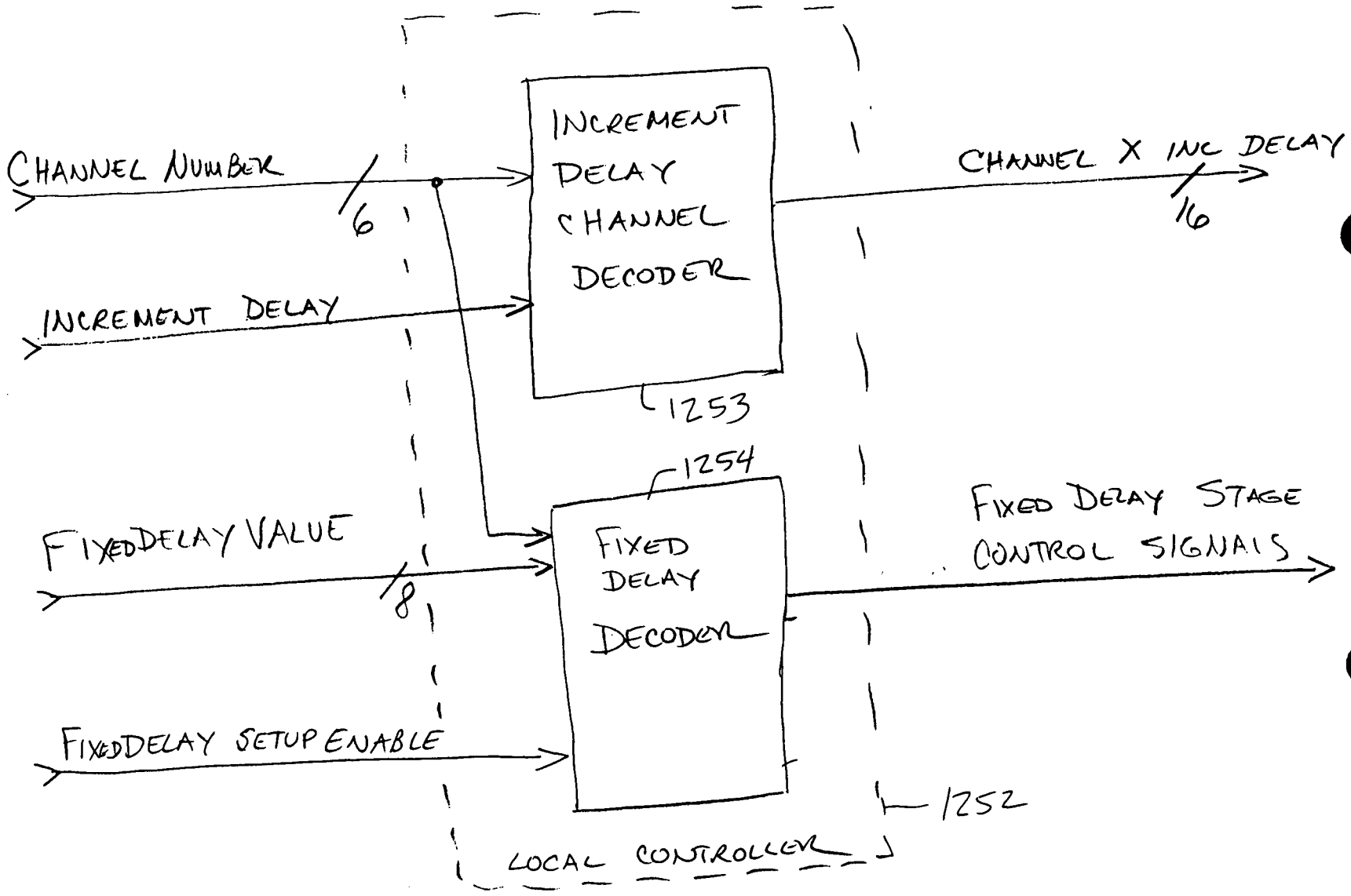


FIG 12R

LEVEL	MAX DELAY LENGTH (CLOCK CYCLES)	NO BITS IN	NO BITS OUT	NO STAGES
1	3	8	9	32
2	6	9	10	16
3	12	10	11	8
4	24	11	12	4
5	48	12	13	2
6	96	13	14	1

FIG 12S

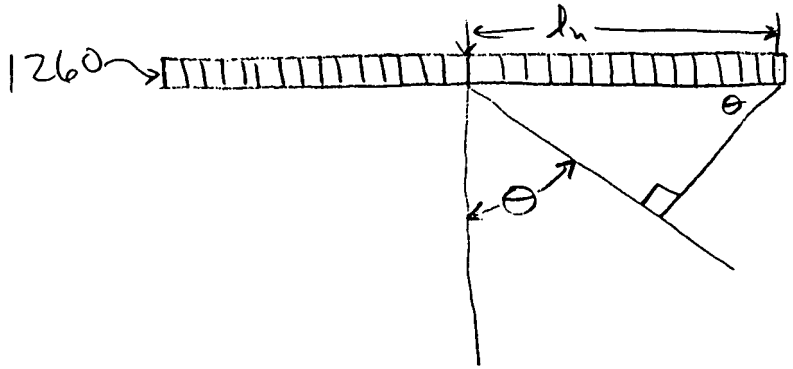


FIG 12T

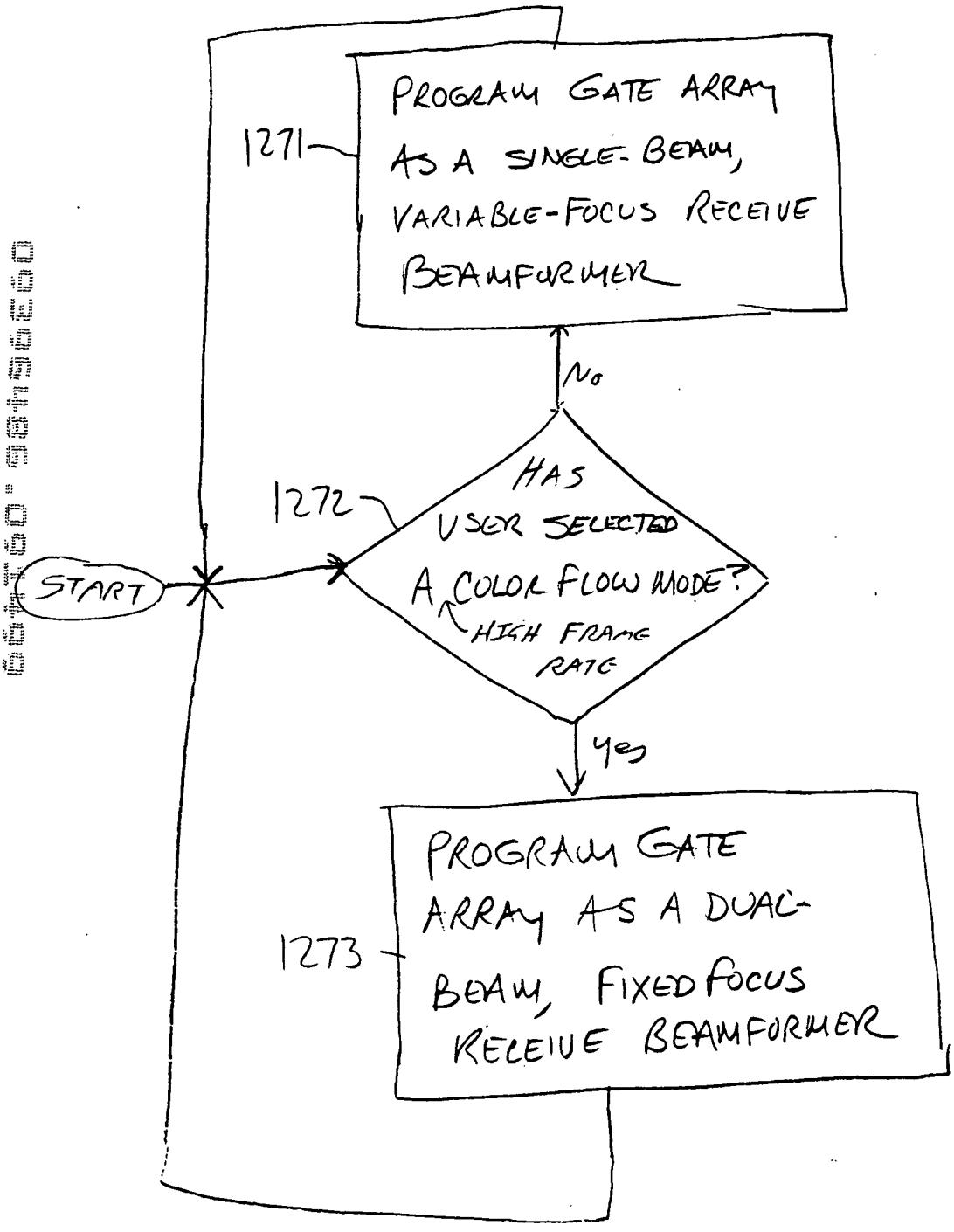

START
1272
HAS USER SELECTED A COLOR FLOW MODE? HIGH FRAME RATE
No
Yes
1271
PROGRAM GATE ARRAY AS A SINGLE-BEAM, VARIABLE-FOCUS RECEIVE BEAMFORMER
1273
PROGRAM GATE ARRAY AS A DUAL-BEAM, FIXED FOCUS RECEIVE BEAMFORMER

FIG 12A

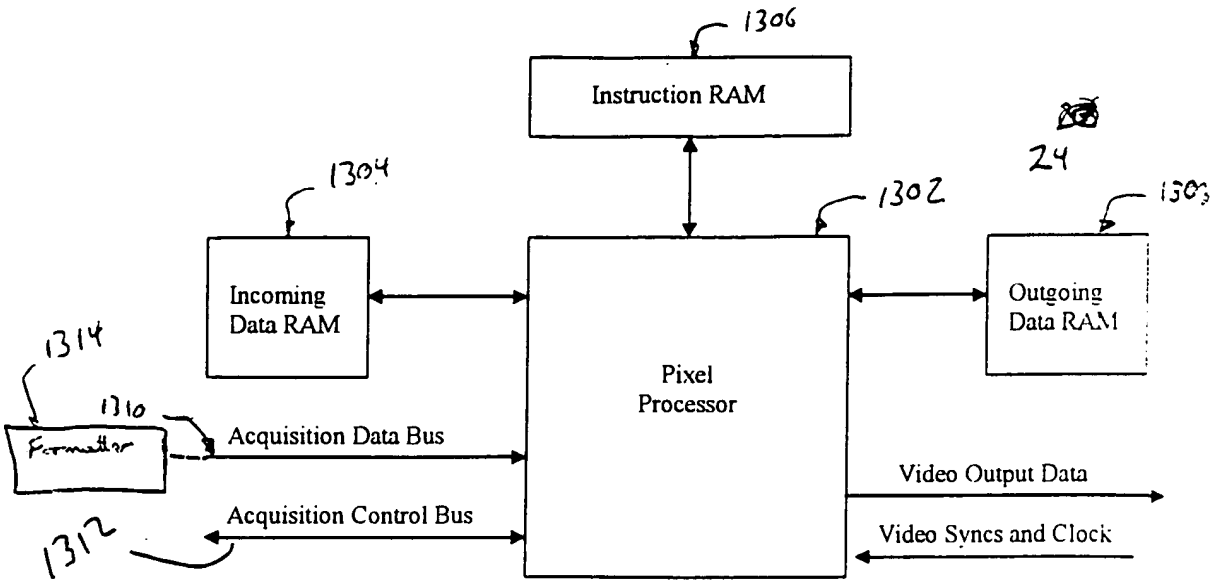

1306
Instruction RAM
24
1304
1302
1303
Incoming
Data RAM
Outgoing
Data RAM
1314
1310
Formatter
Acquisition Data Bus
Pixel
Processor
Video Output Data
Acquisition Control Bus
1312
Video Syncs and Clock

Figure 13A

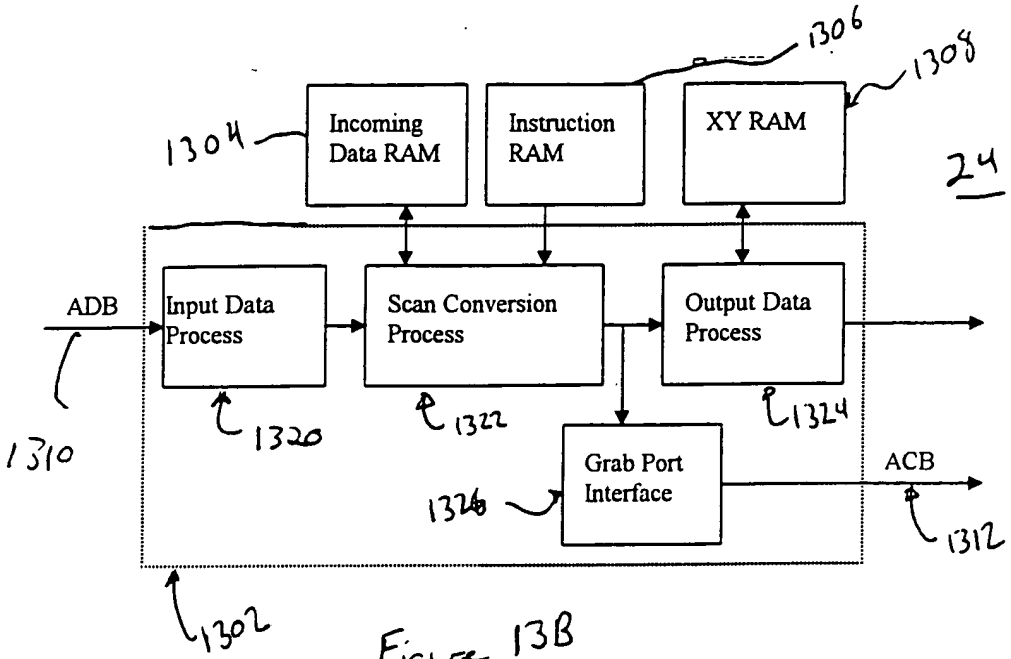

1306
1308
1304
Incoming Data RAM
Instruction RAM
XY RAM
24
ADB
Input Data Process
Scan Conversion Process
Output Data Process
1310
1320
1322
1324
Grab Port Interface
1326
ACB
1312
1302

Figure 13B

Sent by: Sharper

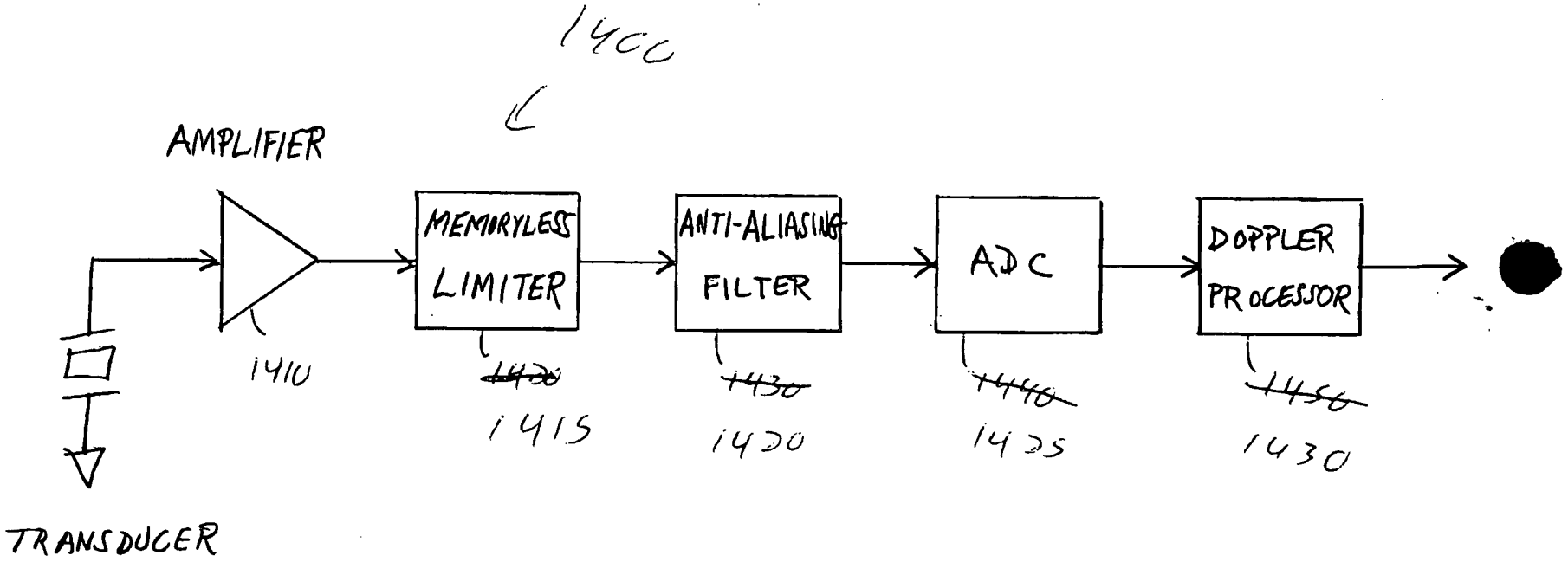


FIGURE ~~6~~ 14